1. Panduranga Vemula[1,2], 2. Rudra Sankar Dhar[1]

Department of Electronics and Communication Engineering, National Institute of Technology Mizoram, Aizawl, 796012, Mizoram, India. (1),
Department of Electronics and Communication Engineering, CMR College of Engineering & Technology, Hyderabad, India (2)
ORCID: 1. 0000-0003-0672-6761; 2. 0000-0002-6571-3808

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Design and Implementation of 6T SRAM Circuitry System using FINFETs

***Abstract**: In the realm of sophisticated VLSI system design, minimizing overall energy dissipation and instantaneous power consumption has emerged as a critical area of focus in recent years. SRAM, with its notable characteristics of high data transfer rates, low power consumption, low supply voltage, and elimination of upgrade requirements, has become the prevalent choice for microprocessor built-in cache memory, game software, computers, and workstations. Consequently, its widespread adoption in portable handheld devices is evident. Adiabatic logic emerges as a promising approach to enhance energy recovery capacity and curtail power dissipation in these circuits, & it allows VLSI circuits to recycle utilised power. In the Adiabatic SRAM good high degree of power reduction is observed. By applying the aforementioned technique same SRAM is investigated by varying technology. In this study, the power values of adiabatic SRAM cells & standard SRAM cells are compared. In contrast to the conventional SRAM cell which is 6T CMOS type, adiabatic logic exhibits superior power and energy efficiency. Leveraging the Cadence® EDA environment, the SRAM cell was meticulously designed, followed by a comprehensive assessment of power and energy consumption across conventional 90nm and 45nm technologies, alongside adiabatic logic in 45nm technology*.

Streszczenie**. W dziedzinie wyrafinowanych projektów systemów VLSI minimalizacja całkowitego rozpraszania energii i chwilowego zużycia energii stała się w ostatnich latach kluczowym obszarem zainteresowania. SRAM, dzięki swoim godnym uwagi cechom, takim jak wysokie szybkości przesyłania danych, niskie zużycie energii, niskie napięcie zasilania i eliminacja wymagań dotyczących aktualizacji, stała się powszechnym wyborem w przypadku wbudowanej pamięci podręcznej mikroprocesora, oprogramowania do gier, komputerów i stacji roboczych. W związku z tym oczywiste jest jego powszechne zastosowanie w przenośnych urządzeniach przenośnych. Logika adiabatyczna okazuje się obiecującym podejściem do zwiększania zdolności odzyskiwania energii i ograniczania jej rozpraszania w tych obwodach, a także umożliwia obwodom VLSI recykling wykorzystanej mocy. W adiabatycznej pamięci SRAM obserwuje się dobry, wysoki stopień redukcji mocy. Stosując wspomnianą technikę, bada się tę samą pamięć SRAM przy użyciu różnych technologii. W tym badaniu porównano wartości mocy adiabatycznych komórek SRAM i standardowych komórek SRAM. W przeciwieństwie do konwencjonalnych ogniw SRAM typu 6T CMOS, logika adiabatyczna charakteryzuje się wyższą mocą i efektywnością energetyczną. Wykorzystując środowisko Cadence® EDA, szczegółowo zaprojektowano ogniwo SRAM, po czym przeprowadzono kompleksową ocenę mocy i zużycia energii w konwencjonalnych technologiach 90 nm i 45 nm, wraz z logiką adiabatyczną w technologii 45 nm.* (Projekt i wdrożenie układu obwodów 6T SRAM z wykorzystaniem FINFET***)

Keywords: VLSI, SRAM(Static Random Access Memory), Adiabatic Logic, CMOS, Power consumption, Sense amplifier.
Słowa kluczowe: VLSI, SRAM(Static Random Access Memory), Adiabatic Logic, CMOS, Power consumption, Sense amplifier.

Introduction

As the prevalence of portable battery-powered systems continues to soar, the need for energy-efficient processors has become increasingly paramount. Energy efficiency is of utmost importance for applications like wearable computing. The batteries in these embedded systems must be repeatedly charged. With wireless sensor networks that are used to monitor environmental data, the issue is more serious. Some systems may not have access to battery charging. We know that the power dissipation of SoC processors is influenced by on-chip memory [1]. Thus, it is crucial to have reliable SRAM, low power, & energy efficiency because it is mostly utilised for on-chip memory.

Various strategies are used to limit power dissipation, including power supply potential scaling and circuit design with power gating. The reduced potential of the power supply causes the dynamic power and leakage power to decrease quadratically and exponentially, respectively [2]. However, scaling up the power supply reduces the noise margin. Numerous SRAM cell designs prioritize minimizing swing potential and active capacitance. In conventional SRAM, power consumption during read operations surpasses that of write operations due to a significantly lower BL potential swing during reads. Approximately total 60% of the overall Dynamic Power taking during read operations stems from power lost in BLs. BL power consumption during write operations is influenced by BL capacitance, the square of the BL potential, and the writing frequency [3].

Limiting potential variations between conducting devices reduces power loss. Voltage waveforms that change over time are used to achieve this. This process is also known as adiabatic charging. The SRAM needs several phase power clocks to operate solely on adiabatic charging principles [4]. To increase the Read noise margin by minimizing the power usage in one bit line static RAM utilizing an adiabatic variation of WL.

SRAM power savings are essential, but caution must also be consider to ensure that main metrics are not significantly impacted. In this operation, efforts were undertaken to utilize & reduce the power that was previously stored in the BLs. To charge & discharge the BLs, a very basic, compact, & effective adiabatic driver was used. The BLs may be charged & discharged according to the input signal thanks to the adiabatic driver's D.C. power clock. As a result, there is far less power lost to the gnd during the "1" to "0" during change over state in SRAM [5].

In adiabatic logic, no separate pre-charging circuit is utilized. As just BLs are used, no synchronization circuit is required. The data is sensed using a low-power sense amplifier. The write driver & the pre-charge circuit must be removed from the traditional SRAM architecture. (Other performance aspects including power, Noise Margin, read & write latency, & power savings are also made possible under various memory operating situations when this adiabatic logic circuit is used with a typical SRAM cell [6]. The impact of the circuit's device characteristics on the power, Read Noise Margin(RNM), & latency of the SRAM cell has been studied [7].

Design and Theory

Adiabatic LOGIC:

By employing adiabatic logic, circuit power consumption is reduced by leveraging energy taking over

from circuit junctions. This concept is embodied in adiabatic logic, a type of low-power VLSI circuit that enables energy reclamation from circuit nodes. The power CLK plays a crucial role in adiabatic circuit operation, with each state of the clock generator dictating the operation of every phase of the adiabatic schematic [8]. As a result, adiabatic circuits exhibit either no or negligible power dissipation due to their inherent properties.

1) The transistor should never be switched on while a potential (VDS > 0) exists between its drain & source.
2) The second one is to never switch off a transistor device if there is a electron flowing through it at any node in time.
3) A diode that is a component of the adiabatic logic should never have currently passed through it.

6T SRAM Cell Design In 14nm FinFET

The adiabatic circuit regenerates energy while the node is in a recovery phase or is discharging from a charged state. In this way, the adiabatic method helps to decreases the overall energy loss and power in the circuit. Integrating this logic into the design of memory cell can save a lot of power in high-density systems. Several adiabatic method schematic controlled by trapezoidal power rails have been described in the given literature [9].

A six-transistor SRAM cell typically comprises four transistors that form two inverters to store a single digital bit of logic 1 and logic 0 data. Two access main transistors regulate the storing and retrieving operations of the storage cell. The core of a main six-transistor SRAM cell with a dual bit line consists of two CMOS inverters, where the output voltage of each inverter feeds back into the input of the other inverter, stabilizing the inverters in their respective states [10].

Input transistors, bitline_bar, word_line, and also bit_line are mainly used to read from or write to the memory cell. Mainly in the standby mode, the WL is less, which turns off the access transistors. At this point, the NOT-gates are in a reverse state. And also when the p-channel MOSFET in the left inverter is on and the p-channel transistor of MOSFET in inverter two is off,voltage at qbar is high, and Q is low. To store information, mainly the data is written to the BL, and the reverse data is written to the inverse bitline, or bit_ line_ bar. The word_ line is then switched to high to activate the access transistors [11]. The inverter transistors may be overridden by the bit_ line driver, which is significantly more powerful. After the data has been stored in the inverters, mainly the access FinFET can be disabled to prevent data loss. The word_line is switched on to turn on the access devices, and the data is sensed at the bitlines [12].

Read Operation

To execute a certain operation in SRAM, the WL must always be high. Memory will be used for performing read operations. Assume Q is 1 & Qb is 0 for memory. The WL is raised for read operations. The output lines are BL & BLB, & these BLs are already pre-charged, i.e. node potential Vdd is present at bit & bit b. There is no potential drop in the circuit since the upper bit is Q. Because Qb is 0 at BLB, there must be a potential differential between Qb & the node potential [13].

As a result, the potential at bit b falls, causing a current flow in the circuit due to the discharge. Because bit & bit b is linked to the sense amplifier, it functions as a estimator. When BLB is less,the sensing amplifier output is one.Assume Q is 0 and Qb is 1 in memory as well [14]. An electrical discharge develops in the schematic at Q and bit as a result of the potential difference. The device should have specified ratios such that Q falls under the P2 specific zone [15]. This is known as the read limitation. As the bit potential lowers, the output is 0. With Q = 0, the output is also 0. As a result, the read operation was successfully confirmed in both circumstances [16].

Write Operation

Vdd is charged to write a '0,' & BL is discharged through the ground. Following these two procedures, WL is set HIGH & data is written into the cell. Consider memory bits with Q is0 & Q is1 values. There are two input lines in the write operation, BL & BLB [17]. To regulate the input lines, first link bit b to the ground, resulting in a large potential difference between Qb & bit b. To write one to the SRAM cell, we must set Q as 1, which may be done by altering the exact ratio of the devices so that pass transistors are stronger than pmos [18]. As a result, Q will be one. Originally, Q is1 following the specific operation, indicating a successful write operation into memory [19].

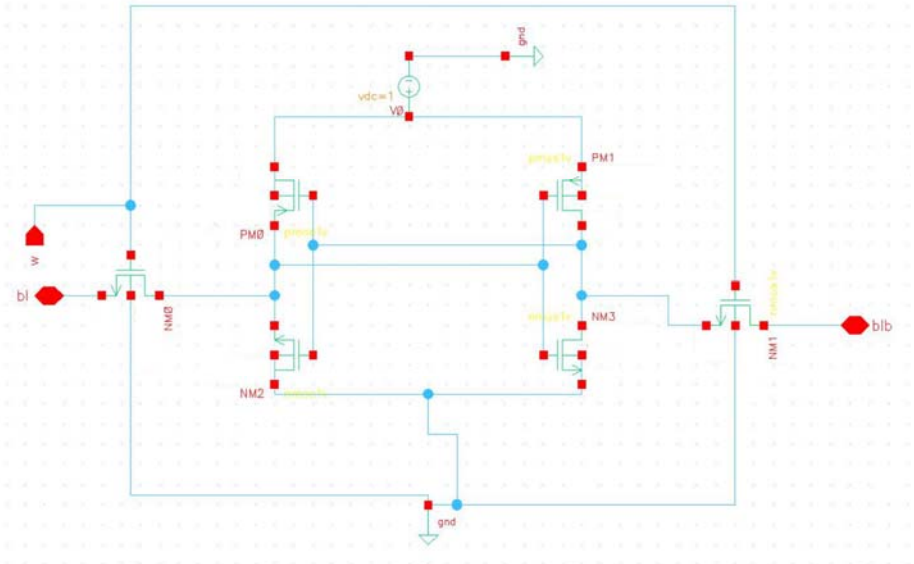

Fig .1. 6T SRAM using MPCL circui

Sense amplifier

The sense amplifier detects the BL & BLB to provide precise monitoring. It improves memory reading speeds while lowering the amount of power required for operation. The sensing amplifier's principal role is to magnify the potential difference created on the BL & BLB during write & read operations [20].

To read "1," which is made up of BL is 1 & BLB is 0, transistors NM2 & NM0 are switched on, while NM1 is switched off, activating PM1 & PM0. This causes VDD to rise at the output logic. When the logic "0" is read using BL=0 & BLB=1, transistors NM1 & NM2 are switched on, while NM0 is switched off, deactivating PM1 & PM0 [21]. As a result, and there is no link between the VDD and output, and the output displays logic "0." The below wave form indicates that the data stored in the BL is read out when se(Sense enable) is strong for a certain period of time [22] .

Proposed model

In write mode, the 6T SRAM cell employed in this design features an adiabatic charging of the BL. According to Figure 1, conventional 6T-SRAM as well as the proposed SRAM cell comprises two switching transistors, MP1 & MN1 (pmos & nmos). With an MCPL (MOS-controlled Power Line) node, several transistors along the rows can share the switching transistors [23]. Through this sharing, the original number of transistors, or in 6T, may be maintained while still achieving adiabatic charging on the BL in writing mode, resulting in a minimal area penalty [24]. In contrast to the nmos, which is linked between the MCPL & ground, the pmos are connected between the power line MCPL & VDD. See Figure.1 to comprehend how the adiabatic SRAM functions [25].

Unlike typical SRAM, logic of mcpl does not require a steady power source. Fig.1 illustrates two key control pins, C1 nd C2. The PMOS transistor connects the power line Vdd to the Modified Complementary Pass Transistor node, while the nMOS transistor connects the ground to the Modified Complementary Pass Transistor (MCPL) node. these control pins, C1 and C2, govern the state of the Modified Complementary Pass Transistor (MCPL) node, which can be either Vdd, ground, or floating depending on the activation of C1 and C2 [20].In Fig.1 When both C1 and C2 are inactive, the PMOS transistor is activated, and the Modified Complementary Pass Transistor (MCPL) node follows Vdd. Conversely, when both S1 and S2 are active, the NMOS transistor is activated, and the Modified Complementary Pass Transistor node follows gnd [26].

In the intermediate state where C1 is active and C2 is inactive, both transistors are turned off, and the Modified Complementary Pass Transistor node becomes floating [27]. This allows the charge from the Bit Lines to charge the Modified Complementary Pass Transistor node through the cross-coupled inverters during the write mode operation, the BL is gradually charged in accordance with the control pins. When C1 is active and C2 is inactive, the bitline charges the q node, while the MCPL remains floating. Once q reaches a state value of '1', p1 is deactivated, and n1 is activated and corresponding schematic has shown in Fig.1. Similarly, if qb is value of '0', p2 is activated, and n2 is deactivated [28] as Shown in Fig.5. This establishes a channel for the charge to flow from the Q node to the Modified Complementary Pass Transistor via p2. In read mode operation, the control pins, c1 and c2, are deactivated, and the SRAM functions as a conventional 6T SRAM, utilizing the Modified Complementary Pass Transistor as the power rail Vdd [29].

Simulation results

4x4 ARRAY LOGIC

Each cell may hold a single bit of binary data. There are four-WLs & four-BLs in this array. Hence, there are a total of 4x4 unique memory blocks in this configuration. Effectively accessing a specific memory cell within this structure requires activating the corresponding WL and BL based on the address received from an external source. Column and row decoders facilitate column and row selection operations, respectively. The row decoder selectively activates one of the four WLs, while the column decoder chooses one of the four BLs. Leveraging a 16-bit RAM, we successfully constructed a 4x4 SRAM Memory Array [30] as shown in the Fig.2 and the corresponding output wave form as shown in Fig.3.

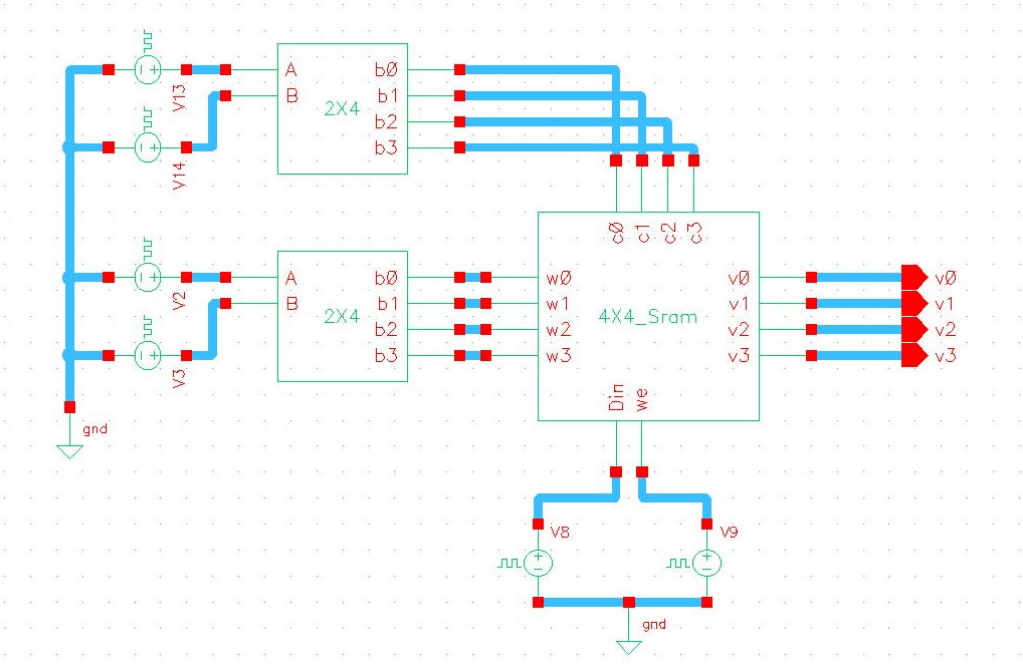

Fig.2. Test circuit for 16-bit (4X4 Array)SRAM

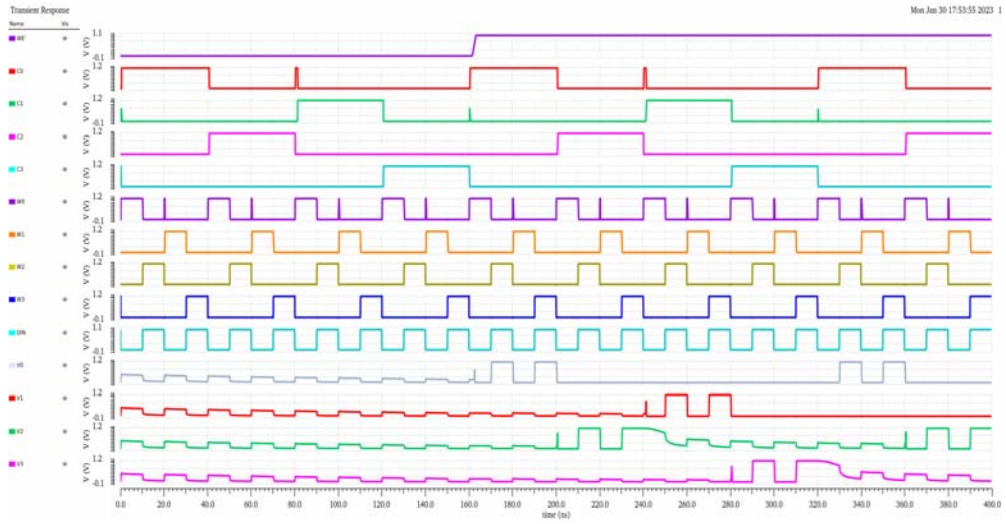

Fig.3. Output for SRAM Memory Array

Table 1: Performance Comparison between Conventional SRAM cell in 45nm,180nm & 6T SRAM Cell using MCPL

Parameter		Conventional 90nm	Conventional 45nm	Adiabatic 14nm (Current Work)
Average Power Consumption	Single Cell	128uW	338nW	258nW
	4X4 Arra	456m	5.6uw	4.4uW
Read Delay		0.02us	0.03ns	0.04ns
Write Delay		0.25us	0.118ns	0.546ns

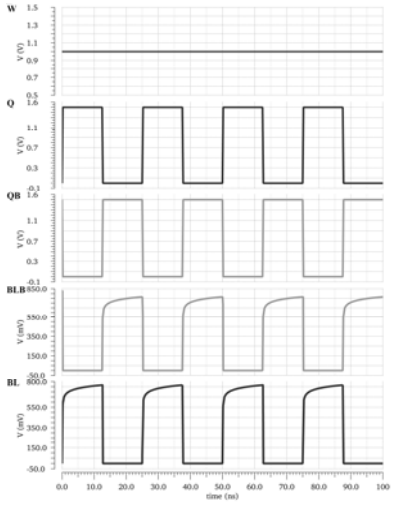

Fig.5.Read Operation.

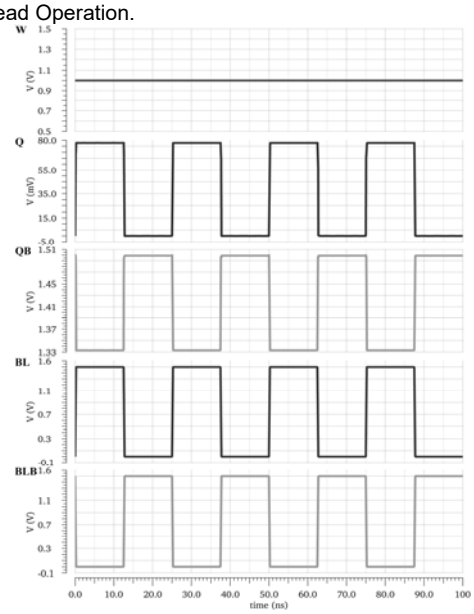

Fig.4.Write Operation.

V The performance Characteristics of the FinFET based 6T SRAM cell and the memory array of the adiabatic logic at 14nm is compared with the conventional SRAM cell at 45nm and 90nm and the corresponding Out put Wave form of a Memory array was shown in Fig.3.The Power Consumption of the FinFET based memory cell and memory array is less with the conventional memory cell. The characteristics are compared in the Table.1 and the read delay and write delay is also compared. The average power consumption of single cell and the memory array of SRAM is compared in the Table.1 and During the write operation the Data is stored in cell as shown in Fig.4 and also during cell read operation the data is retrieved as shown in Fig.5

Conclusion

This paper describes the implementation of an 6T Static RAM memory cell at 14nm advanced FinFET Technology. The implementation was completely by choosing consistent results at various states of memory write operation and memory retrieve operations. This method also includes a exact estimation of conventional 6T and also 8T SRAM cells based on various well-implemented FinFET devices in the sub-14nm region and also compared with 45nm and 90nm.

Adiabatic logic has been successfully integrated into the 6T SRAM architecture, yielding a low-power alternative to conventional SRAM. Comprehensive evaluations across various technological nodes demonstrate the proposed SRAM's superior power efficiency compared to its conventional counterpart. A 4x4 memory array has been meticulously designed and rigorously tested for both read and write operations.

REFERENCES

[1] Shreelakshmi, Sendamarai P “Enhancement of Design Quality for an 8-bit ALU” ABHIYANTRIKI an international journal of engineering & technology (AIJET) Vol. 3, No. 5,May 2016.

[2] NahidRahman, B. P. Singh “Design and Verification of Low Power SRAM using 8T SRAM Cell Approach”,an International Journal of Computer Applications.Volume 67,No.18, April 2013.

[3] T.Paridhi Athe,S.Dasgupta,"A Comparative Study of 6T,8T and 9T Decanano SRAM cell" 2009 IEEE Symposium on Industrial Electronics and Applications,Vol-2,October 4-6,2009.
[4] S. Birlaeta., "Static Noise Margin Analysis of Various SRAM Topologies", IACSIT, vol.3, No.3, June 2011.
[5] Premalatha, "A Comparative Analysis of 6T, 7T, 8T and 9T SRAM Cells in 90nm Technology" 2015 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT) 27 August 2015.
[6] Kirti Bushan Bawa, "A Comparative Study of 6T, 8T and 9T SRAM Cell" Volume 3,Issue 6, June 2015.
[7] D. Burnett, K. Erington, C. Subramanian, & K. Baker, "Implications of fundamental threshold potential variations for high-density SRAM & logic circuits," in Proc. Symp. VLSI Tech, pp. 15–16,1994.
[8] V. Gupta & M. Anis, "Statistical design of the 6T SRAM bit cell," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 1, pp. 93–104, Jan. 2010.
[9] Mansi S. Warde, V. Chandana S "Design & Analysis of 8x8 Static RAM", International Journal of Scientific & Engineering Research, Volume 6, Issue 7, July-2015.
[10] A. Blotti & R. Saletti, "Ultralow-power adiabatic circuit semi-custom design," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 11, pp. 1248– 1253, Nov. 2004.
[11] Pandu Ranga Vemula,Rudra Shankar Dhar"Design of 8T SRAM using 14nm FinFET Technology" Przegląd Elektrotechniczny, ISSN 0033-2097, No. 98 ,2022.
[12] Yasuhiro Takahashi, Nazrul Anuar Nayan, Toshikazu Sekine, Michio Yokoyama,"Low-power adiabatic 9T static random access memory" The Journal of Engineering; published by the IET,vol.2014,Issue 6, pp. 259–264, April 2014.
[13] V. S. Kanchana Bhaaskaran"Energy Recovery Performance of Quasi-Adiabatic Circuits using Lower Technology Nodes", IICPE, 2010.
[14] E. Seevinck, F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," IEEE J. Solid-State Circuits, vol. 22, no. 5, pp. 748–754, Oct. 1987.
[15] Chotaro Masuda, Tetsuya Hirose, Kei Matsumoto, Yuji Osaki, Nobutaka Kuroki, & Masahiro Numa, "High Current Efficiency Sense Amplifier Using Body-Bias Control for Ultra-Low-Voltage SRAM", in Circuits & Systems (MWSCAS),2011 IEEE 54th International Midwest Symposium,2011.
[16] Behzad Ebrahimi, Saeed Zeinolabedinzadeh, AliAfzali-Kusha:Low Standby Power and Robust FinFET Based SRAM Design, IEEE Computer Society Annual Symposium on VLSI,2008.
[17] Evert seevinck, senior member, IEEE, Frans j. List, and Jan lohstroh,"Static-Noise MarginAnalysis of MOS SRAM Cells" IEEE Journal of solid-state circuits, vol-22,Issue-No. 5,1987.
[18] A Priydarshi.et.al, "Low-Power and High-Speed Technique for logic Gates in 20nm Double-Gate
FinFET Technology", Journal of Physics: Conference Series 755,012055,October 2016.
[19] S.H. Kim and J.G. Fossum, "Design Optimization and Performance Projection of Double-Gate FinFETswith Gate-Source/Drain Underlap for SRAM Application," IEEE Trans.
Electron Devices, vol. 54, no. 8, pp. 1934–1942, August 2007.
[20] R.V. Joshi, R.Q. Williams, E. Nowak, K.Kim,J.Beginner, T.Ludwig, I.Aller, and C. Chuang, "FinFET SRAM for HighPerformance LowPower Applications," ESSCIRC, 2004, pp. 211-4.
[21] Kohlolhal, Ranjit, and Vanita Agarwal. "A Power and Static Noise Margin Analysis of different SRAM cells at 180nm Technology." In 2019 3rd International Conference on Electronics, Communication and Aerospace Technology (ICECA), pp. 6-12. IEEE, 2019.
[22] Budhaditya Majumdar, Sumana Basu, "Low Power Single Bit line 6T SRAM Cell With High Read Stability", IEEE 2011 International Conference on Recent Trends in Information Systems,Pp.169-174, February-2012
[23] E. Grossar, "Read Stability and Write-Ability Analysis of SRAM Cells for Nanometer Technologies", IEEE Journal of Solid-State Circuits, vol.41, no.11, pp. 2577-258, Nov.2006.
[24] S. Nanda, and R. S. Dhar, "Exploration and Development of TG Quantum Well Barrier FinFET with Strained HOI Nanosystem Channel for Enhanced Performance", Computers & Electrical Engineering Journal, Elsevier, Vol. 98, pp. 107687-1-13, January 2022.
[25] K. Kumar, and R. S. Dhar, "Exploration of improved leakage based performance analysis for underlap induced strained-Si layer in tri-layered channel DG nanoFETs", Physica Scripta Journal, IOP, Vol. 96, pp. 124006-1-10, December 2021, ISSN: 1402-4896.
[26] S. Hungyo, R. S. Dhar, K. Kumar, K. J. Singh, R. Dey, and S. Bhattacharya, "Estimation and analysis for modelling of stand-alone graphene/AlGaAs/GaAs schottky solar photovoltaic cell module for power conversion efficiency", Microsystem Technologies Journal, Springer, Vol. 27, Issue 10, pp. 3693–3701, October 2021, ISSN: 1432-1858.
[27] J. S. Tamang, R. S. Dhar, A. K. Bhoi, A. K. Singh, and S. Chatterjee, "Bio-Sensing Application of Chalcogenide Thin Film in a Graphene-Based Surface Plasmon Resonance (SPR) Sensor", Sadhana Journal, Indian Academy of Sciences, Springer, Vol.46, No.120, pp.120-1-10, June 2021, ISSN: 0973-7677.
[28] Szcześniak A., Szcześniak J., Application of read-only memory to conversion of signals of optoelectronic position transducer, Przegląd Elektrotechniczny, 7 (2014), 84-87.
[29] Dlugosz R.T., Talaska T., Wojtyna R., An influence of current-leakage in analog memory on training Kohonen neural network implemented on silicon, Przeglad Elektrontechniczny (Electrical Review) 86 (2010), no. 11a, 146-150.
[30] Waśkiewicz J., Gołębiowski J., Resistive memory physical mechanism in a thin-film Ag/YBa2Cu3O7-x/Ag structure, Przegląd Elektrotechniczny, 91 (2015), no. 11, 313-317.