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A low-power 100MS/s Flash ADC with Thermometer code encoding technique for automotive applications

Abstract. *A 3-bit 100MS/s flash Analog-to-Digital Converter (ADC) with thermometer code encoding technique is proposed. A novel XOR-based thermometer to a gray encoder and clocked PMOS-based dynamic comparator is designed. Flash ADC design compares the input voltage to a predetermined reference value using comparators to produce a gray code output. To improve the power efficiency PMOS based dynamic comparator is used. Conventional Dynamic latched comparators suffer from kickback noise, which lowers the performance of Flash ADC. To overcome this problem, a new architecture of dynamic latched comparator with PMOS technique is designed. The proposed Flash ADC uses the conversion of thermometer to gray coding to reduce the bubble errors. Based on the simulation results the proposed Flash ADC consumes 2.4mW of power when operating at 100 MHz and a 1.8 V power supply. The proposed flash ADC achieves excellent accuracy and low power consumption by utilizing a novel thermometer code encoding technique.*

Streszczenie. *Zaproponowano 3-bitowy 100MS/s flash Analog-to-Digital Converter (ADC) z techniką kodowania kodu termometru. Zaprojektowano nowy termometr oparty na XOR do enkodera Graya i taktowanego komparatora dynamicznego opartego na PMOS. Projekt Flash ADC porównuje napięcie wejściowe do ustalonej wartości odniesienia za pomocą komparatorów w celu wygenerowania wyjścia kodu Graya. Aby poprawić wydajność energetyczną, zastosowano komparator dynamiczny oparty na PMOS. Konwencjonalne komparatory dynamiczne z zatrzaskiem są narażone na szum odrzutu, który obniża wydajność Flash ADC. Aby przezwyciężyć ten problem, zaprojektowano nową architekturę komparatora dynamicznego z zatrzaskiem z techniką PMOS. Proponowany Flash ADC wykorzystuje konwersję termometru na kodowanie Graya w celu zmniejszenia błędów pęcherzyków. Na podstawie wyników symulacji proponowany Flash ADC zużywa 2,4 mW mocy podczas pracy przy 100 MHz i zasilaniu 1,8 V. Proponowany flash ADC osiąga doskonałą dokładność i niskie zużycie energii dzięki wykorzystaniu nowatorskiej techniki kodowania kodu termometru.* (***Przetwornik ADC Flash o niskim poborze mocy 100 MS/s z techniką kodowania kodu termometru do zastosowań motoryzacyjnych***)

Keywords: Clocked PMOS technique; Dynamic Latch Comparator; Flash Analog-to-Digital Converter ; Thermometer code encoding technique;
Słowa kluczowe: echnika zegarowego PMOS; Komparator dynamicznego zatrzasku; Przetwornik analogowo-cyfrowy Flash; Technika kodowania kodu termometru;

IntroductionN

Flash ADCs can do conversions at high speeds using just one channel. As a result, flash ADCs continue to be appealing for high-speed applications. Flash ADCs, have a fundamental flaw in that they are burdened by an exponentially growing number of comparators. The demand for good performance converters has expanded. Although the cascaded latch interpolation technique is conceptually simple, it also raises many problems[1,31]. The input and reference voltages are converted by the charge Pump into different ramp signals that are sent to comparators. The Dickson Charge Pumps' built-in input voltage boosting allows the ADC to give the widest possible bandwidth [2,32]. Time domain latch interpolation reduces power consumption [3]. The RNS (Remainder Number system) quantization boosts the flash ADC's figure of merit [4]. To speed the conversion, vernier time-to-digital converters are pipelined. The residue transfer is accomplished by a charge-steering amplifier [5]. Equations for calculating bandwidth are provided by the track-and-hold circuit and subsequent buffer stage [6]. High resolution can be attained by operating the complimentary dynamic amplifiers in a dual-edge fashion [7]. Bootstrapped circuit, Switch Unit, DAC, Fine ADC (5-bit), and Coarse ADC (2.5-bit) components all consume 6.8 mW while employing the Interpolation technique and Sample-and-Hold Sharing Technique. Timing skew error occurs when the same clock signal from the same source arrives at various components at various times. Due to an accidental departure from a target value, there is an offset mismatch [8,33]. The digital encoder consumes 2.898 mW and the Comparator array consumes 10.6 mW while utilizing the Cascaded Latch Interpolation Technique.1.44 ps rms of sampling skew are required [9]. Components like Bootstrapped track and hold, Resistor string, voltage-to-time converters (VTC) array, time-domain interpolation (TDI) array, SR latches (SRL) array, Thermometer Grey - Binary Code Encoder, Clock Generator, and others require 7.5mW while utilizing Time-Domain Interpolation Technique. Errors in the slope and residual offset occurred [10]. Utilizing the interleaved method, the power used is 0.4 W. Due to high distortion, the SNDR has been degraded [11]. utilizing the Time-Domain method Power use is 21 mW.

The input capacitance and (Voltage-to-Time) conversion gain limits the ERBW (Effective Resolution Bandwidth), while the LSB size of the TDC (Time-to-Digital converter) is dependent on supply voltage and temperature [12].ADC core size and power consumption are reduced by using a two-stage cascaded latch interpolation technology [13]. To increase ADC metastability tolerance, a selection technique is used in a time-interleaved-based ADC [14]. The sub-R function is implemented by digital-sub-ranging-R, which reduces the latency between coarse and fine conversions [15]. Bootstrap track-and-hold circuit based on source followers to decrease input kickback and enhance ADC bandwidth [16,34]. Using an offset-cancelling charge-steering amplifier and an analog-centric approach offered to decrease power wastage [17]. Using asymmetrical track and hold timing, the two-step sub-ranging ADC architecture enables coarse and fine conversions in a single sample clock cycle [18]. In addition to increasing the input bandwidth, a top-plate sampling circuit also removes the gain error of the ADCs [19,35]. To further reduce the comparator noise, a modified Strong-ARM latch is used [20]. To drastically cut the power consumption capacitor DACs are employed as the reference selection circuit. To lower offset voltage, the comparators additionally use a gate-weighted interpolation approach [21].

Conventional methods

Flash ADC is proven to be the highest-speed ADC and it is useful for high computing applications.Fig.1. shows the basic block diagram of a conventional Flash ADC.

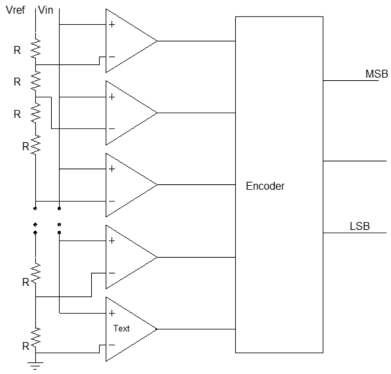


Fig.1. Basic architecture of conventional Flash ADC

The conventional Flash ADC comprises of comparators, resistor ladder network and a digital encoder circuit. The reference voltage is taken from the voltage traps of the resistive ladder network. The comparators used in the ADC are used to provide the digital output by comparing the input analog voltage with the reference voltage. The encoder is used to produce binary codes. Based on the resolution of ADC a designer can select the number of comparators. Therefore, 2N-1 comparators are required to design the ADC and the complexity of the ADC increases. To save the required amount of power, a clocked PMOS-based Dynamic latched comparator is designed in the flash ADC.

A dynamic comparator may do numerous comparisons quickly and repeatedly by using a feedback network and storing the output voltage in a latch or flip-flop, without a significant number of complex logic gates[36-38]. Normally, the conventional static latched comparator suffers from kickback noise. This generated kickback noise disturbs the input analog signal and introduces errors in the comparator circuit. To overcome the kickback noise effect the designed flash ADC comprises a novel thermometer to a gray encoder and clocked PMOS-based Dynamic latched comparator. The comparator's speed and accuracy are increased via the feedback network. Inn, Inp, Vss, Vdd, and clk are the input signals of the Dynamic latched comparator. Inn and Inp are used to provide a reference signal and analog input signal. Through Vdd, the supply voltage appropriate to the technology node is provided. The output is indicated by the pins Outn and Outp.Fig.2. shows the conventional Dynamic Comparator.

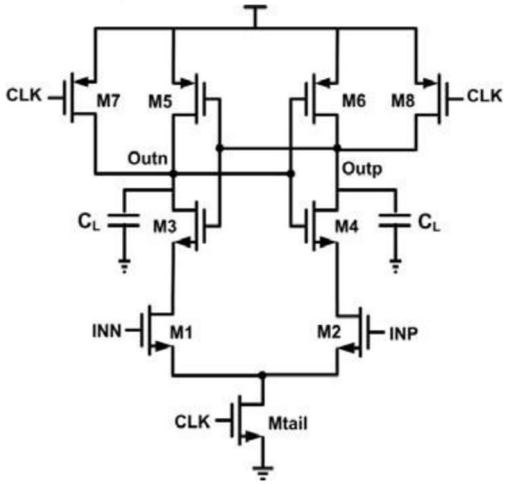


Fig.2. Circuit diagram of Dynamic Comparator circuit [22]

Proposed methodology

The proposed ADC consists of PMOS based Dynamic latch comparator, resistor ladder network and thermometer to gray code encoder.Fig. 3. shows the circuit diagram of the proposed flash ADC.

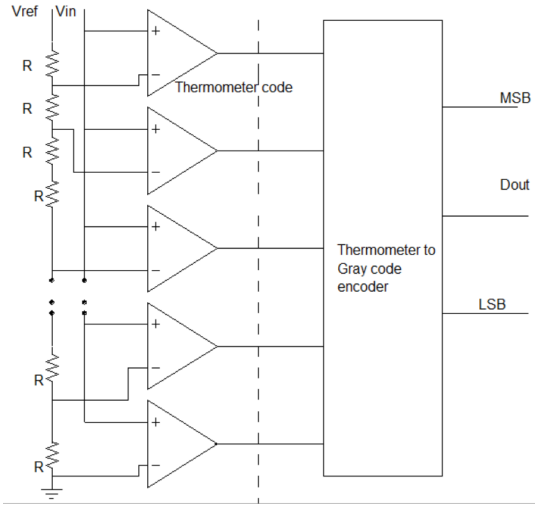


Fig.3. Basic architecture of the proposed Flash ADC

3.1. XOR gate based on Transmission Gate Logic:

Fig.4. represents the circuit diagram of the transmission gate logic-based xor gate. A and Abar, B and Bbar are complement to each other. When the A=0, B=0, then the output Y=0.When A=0, B=1, then the output Y=1. Both PMOS and NMOS transistors are good transmission of logic '1' and logic '0'.

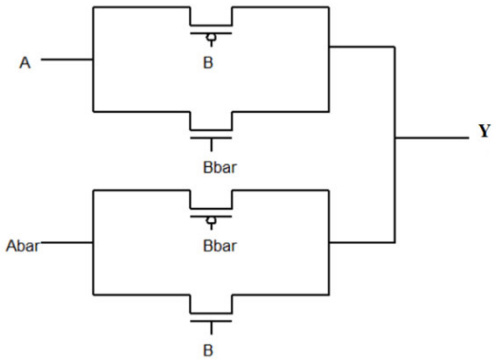


Fig.4. Schematic of xor gate with transmission gate logic.

3.2. Proposed Thermometer-to-gray Code Encoder.

A thermometer-to-gray encoder is designed with transmission gate logic to convert a thermometer code into a gray code. The below equations serve as its implementation.

(1) G3=T4

(2) G2=T2 xor T6

(3) G1=(T1 xor T3) + (T5 xor T7)

Fig.5. shows circuit diagram of the Thermometer to Gray Encoder.T1- T7 are the inputs and G1-G3 are the outputs.

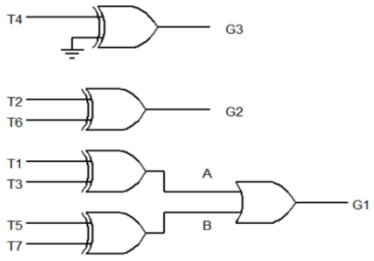


Fig.5. Schematic of Thermometer to Gray Encoder

The thermocode output from the Dynamic Comparator is converted into gray code using the encoder. The gray codes are obtained using the following equations.

G3=T4^ 0 (4)

G2=T2^ T6 (5)

G1=T5 ^T7 + T1^T3 (6)

3.3. PMOS based Dynamic Latch Comparator

The Fig.6. shows the PMOS based Dynamic latch comparator operates in two phases. During reset phase, the input clk=0 and M1,Mtail1 transistors turn OFF. This condition reduces the static power consumption. Both the transistors M4 and M5 pulls the tn and tp to VDD and the transistors MR1 and MR2 transistors pulls the latch outputs to zero potential. When the input clk =1, both the tail transistors turns ON and M4 and M5 pulls the tn and tp nodes to Vss and a differential voltage based on the input potential is developed (Vdiff). The middle transistors MR1 and MR2 provides this differential voltage to the cross coupled Complementary Metal Oxide Semiconductors (CMOS) which provides a provides a proper isolation between the output and the input signal. The kick back noise is gradually decreased by clocked PMOS transistor. The main purpose of the PMOS transistor is to increase the node Voltage to Vdd by setting the clock input signal to low level.

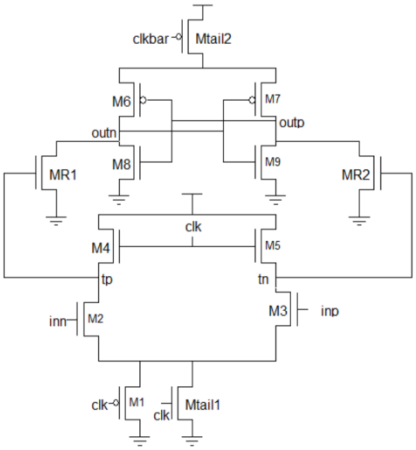


Fig.6. Circuit diagram of clocked PMOS Dynamic latch Comparator

Resultsm and discussion

The flash ADC is designed using 100-MS/s conversion rate with a thermocode technique in a CMOS process. Various sub-blocks including Dynamic latch comparator,Thermometer to gray code converter and resistive ladder network with various reference voltages are simulated.Fig.7. shows the output waveform of the dynamic comparator circuit. Outn is the output, whereas Vin, Vref, and Clk are the inputs. The analog input signal and the reference voltage is compared and if the analog signal is greater than the reference voltage the comparator output is1. If the analog signal is lesser than reference voltage the comparator output is 0. The digital output of the comparator is given to encoder to produce the digital output.

Fig.8. shows the output of the xor gate .If the two inputs are different, it produces a logic high(1) as output. If two inputs are the same, it produces logic low(0) as output.

The output waveform of the thermometer to the gray encoder is shown in Fig.9. When the inputs T1-T7 are high ,then the obtained output is 100.The vertical marker in Fig.9. shows that when the input T1 alone is high, the output is 001.

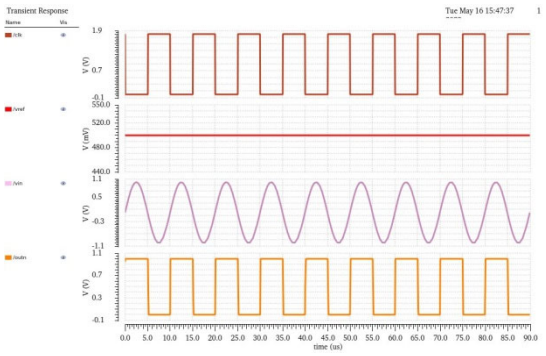


Fig.7. Output waveform of Dynamic Comparator circuit

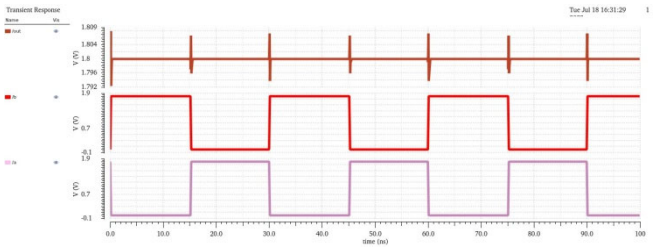


Fig.8. Output waveform of XOR circuit

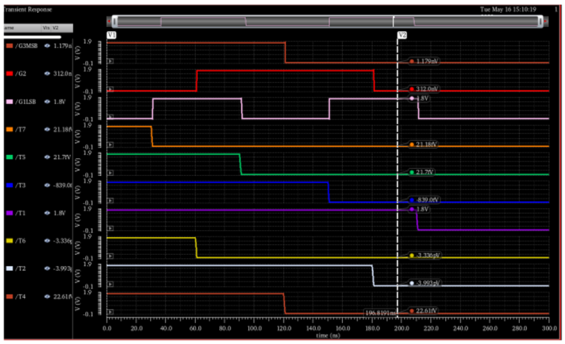


Fig.9. Output waveform of the thermometer to gray encoder

In Fig.10, the flash ADC circuit's output waveform is shown. Inputs to the flash ADC are Vin, Vdd, Vref, Vss, and clk signals. The input analog signal of 2V is given to the Vin of the comparator. It is compared with the reference signal and the output is displayed through MSB, LSB, and G2 pins. The output is 100 when all inputs are high. The output is 011 as a result of the slow transition happens between T1 and T2 signals.

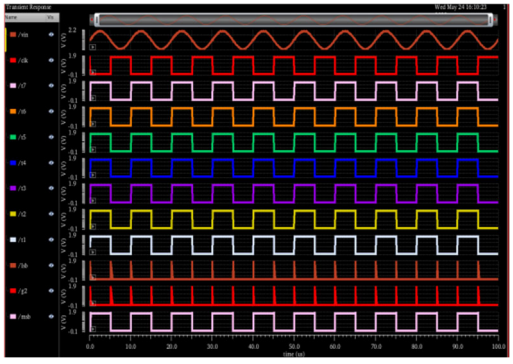
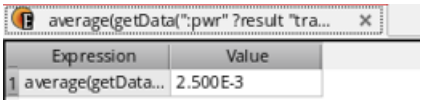
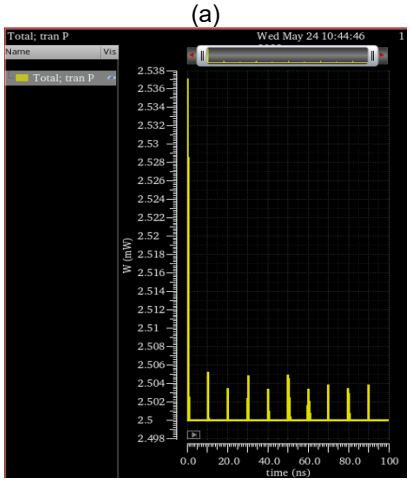


Fig.10. Output waveform of Flash ADC circuit

Fig.11.(a) shows the average power consumption of flash ADC. Fig.11.(b) depicts the power consumption of Flash ADC. The obtained power of the proposed Flash ADC is 2.5mW in a 45nm CMOS process.



(a)



(b)

Fig.11. (a) Average power and (b)power waveform of flash ADC circuit

The IC6.1.8 version of the Cadence Virtuoso software yields the results listed below. TABLE 1. compares the performance of comparators. At a frequency of 2 MHz, the double tail dynamic comparator has a power and delay of 97 nW and 75 ps. The dynamic comparator's power and delay are 512.2 nW and 505.7 ns. The output accuracy is good in the dynamic comparator so at a frequency of 100 MHz, the dynamic comparator is used.

TABLE 1. Performance analysis of the comparator with power, speed, and delay parameters.

S.N	Component	Average	Tp_HL	Tp_LH	Total Pr	Freq
1.	Double Tail Comparator	97.71 nW	75 ps	75 ps	75 ps	2
2.	Dynamic comparator	512.2 nW	-450.3 ns	-55.4 ns	505.7 ns	2
3.	Dynamic Latch comparator	6 µW	9.76 ns	4.7 ns	14.46 ns	100

TABLE 2. shows the comparative analysis of the XOR gate with other techniques. XOR gate is designed using Pass transistor logic, Transmission gate logic, and Conventional logic. The power consumption of XOR logic using Pass transistor logic is 88 nW. The power consumption of XOR logic using Transmission gate logic is 138.8 nW. However, the power obtained by the conventional logic is 1260 nW. The power consumption is greatly reduced by adapting the Transmission gate logic which proves with less power consumption.

TABLE 2. Performance analysis of the xor gate with power.

Component	Techniques	Average Power (nW)
XOR gate	Transmission gate logic	138.8
	Conventional logic	1260

TABLE 3. compares the performance of two different encoders. The power consumption of Priority encoder and thermometer to gray encoder is around 15.9 µW and 4.3 µW. The proposed Flash ADC is designed with a low-power thermometer to gray code encoder logic.

TABLE 3. Performance analysis of the encoder with power, speed and delay parameters.

S.N	Component	Average	Tp_HL	Tp_LH	Total Pr
1.	Priority Encoder	15.19 µW	0.03	-0.031	0.141
2.	Transmission gate logic based Thermometer to Gray Encoder	4.3 µW	59.2	-119.7	60.5

TABLE 4. compares the different techniques used in the flash ADC based on power consumption. The power of the proposed thermometer coding technique is less when compared to all other techniques and the output is accurate. Hence the designed 3-bit,100MSPS Flash ADC consumes 2.5mW of power, and the high-performance Flash ADC can be used for automotive applications.

TABLE 4. Performance analysis of the flash adc.

Component	Technique	Average Power (mW)
Flash ADC	Interpolation [24]	6.8
	Cascaded Latch Interpolation [25]	20.7
	Time-Domain Interpolation[26]	7.5
	Interleaved [27]	400
	Time-Domain Remainder Number System Quantization [28]	21
	Time-domain Latch Interpolation [29]	15.1
	Proposed Thermocode Technique	2.5

Conclusion

In this work, a 3-bit 100MSPS Flash ADC with thermometer code encoding technique is presented. To reduce the kickback noise effect a PMOS-based Dynamic latch comparator is proposed in this work. Different comparators and encoders' power, speed, and delay are investigated. At a frequency of 2 MHz, the double tail dynamic comparator has a power and delay of 97 nW and 75 ps. At a frequency of 100 MHz, the power consumption and delay of the dynamic comparator are 6 µW and 14.46 ns, respectively. The power consumption of Priority and thermometer to gray encoder are 15.9 µW and 4.3 µW. Priority encoder and thermometer to gray encoder have a delay of 0.141 ns 60.5 ns, respectively. Comparing various techniques, the proposed thermometer encoding code technique consumes less power of 2.5mW in a 90nm CMOS process. Based on the performance the proposed ADC can be used for automotive applications.

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