1. Chandralekha Mohanachandran [1], 2. Srinivasan Sumathi [1]

RNS Institute of Technology, Bengaluru 560098, India (1)
ORCID: 1.0000-0003-3803-1630; 2.0000-0002-5730-0608

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Performance Evaluation of Forward Error Correcting Codes for Design of Power Line Carrier Communication Modem

***Abstract**. An analysis of three coding schemes, Reed-Solomon code, the Viterbi decoded convolutional code and the concatenated Reed-Solomon – Convolutional code for power line carrier communication is presented in this article. The simulation results are validated using theoretical bounds for all mapping schemes specified in standard IEEE STD 1901.2. The theoretical and analytical result shows that the performance of inner convolutional code with outer Reed-Solomon code is the superior coding scheme with benefits such as improved bit error rate performance, better burst error correcting capability and greater redundancy.*

***Streszczenie.** W artykule przedstawiono analizę trzech schematów kodowania kodu Reed-Solomon, dekodowanego Viterbiego kodu splotowego oraz połączonego kodu Reed-Solomon-Convolutional dla komunikacji nośnej w sieci energetycznej. Wyniki symulacji są sprawdzane przy użyciu teoretycznych granic dla wszystkich schematów mapowania określonych w standardzie IEEE STD 1901.2. Teoretyczne i analityczne wyniki pokazują, że wydajność wewnętrznego kodu splotowego z zewnętrznym kodem Reeda-Solomona jest lepszym schematem kodowania z korzyściami, takimi jak lepsza wydajność bitowej stopy błędów, lepsza zdolność korekcji błędów seryjnych i większa redundancja. (**Ocena wydajności kodów korekcji błędów przewodzenia do projektowania modemu komunikacyjnego linii elektroenergetycznej**)*

Keywords: IEEE STD 1901.2, Reed-Solomon, Convolutional, Concatenated code.
Słowa kluczowe: IEEE STD 1901.2, Reed-Solomon, splotowy, kod połączony.

Introduction

Efficient control and management of electric power generation, transmission and distribution require a reliable communication system. Power line carrier communication (PLCC) offers a cost-effective medium where a high-frequency carrier signal is superimposed on the existing power transmission line for data transmission. In the field of smart grids, PLCC finds application in fault identification and reporting system [1], automatic meter reading (AMR) [2] and demand-based management systems [3]. By adopting the advanced digital signal processing technology into PLCC, it is possible to make the system flexible, economical and reliable. As more and more manufacturers worldwide are expected to develop innovative PLCC systems and share the same power grid, it is required for the developer to follow a standard which offers interoperability. IEEE STD 1901.2 is one such standard for frequency range up to 500kHz used in smart grid for PLCC. The standard specifies the data packaging, noise cancellation methods, and modulation techniques and offers a coexistence mechanism [4].

IEEE STD 1901.2 lists BPSK, QPSK, 8PSK, DBPSK, DQPSK, D8PSK and 16QAM as the types of mapping to implement in the modem design [5]. Bit Error Rate (BER) performance degrades with an increase in modulation order [6] and thus an adaptive mapping system where the best modulation scheme is chosen according to varying channel conditions is a requirement. The decision-making algorithm for adaptive mapping is implemented in the models presented in this article.

Forward error correcting (FEC) codes are employed in wireless communication systems to correct random and burst errors perceived at the receiver [7], these innovations contribute to an improvement in error correcting codes in PLCC. This paper presents the BER performance of the Viterbi decoded convolutional code, Reed-Solomon (RS) code and the concatenated RS – Convolutional code for all mapping schemes listed in IEEE1901.2 standard.

Viterbi decoded convolutional coding model design

The systems are modelled using the SIMULINK application in the Matlab platform. The proposed flowchart of the adaptive modulation is shown in figure 1. Based on the threshold set for Signal to Noise Ratio (SNR) the adaptive decision-making algorithm shall automatically choose the appropriate mapping scheme. In the model illustrated in figure 2, three parallel paths originate from the encoder and feed three different types of mapping – coherent Phase shift keying (PSK), differential PSK, and quadrature amplitude modulation (QAM). During the operation, one path will only be active. A software-driven multipath switch operates according to the output of the adaptive decision algorithm based on the number of states (M) in the mapping constellation and the type of mapping (Coh).

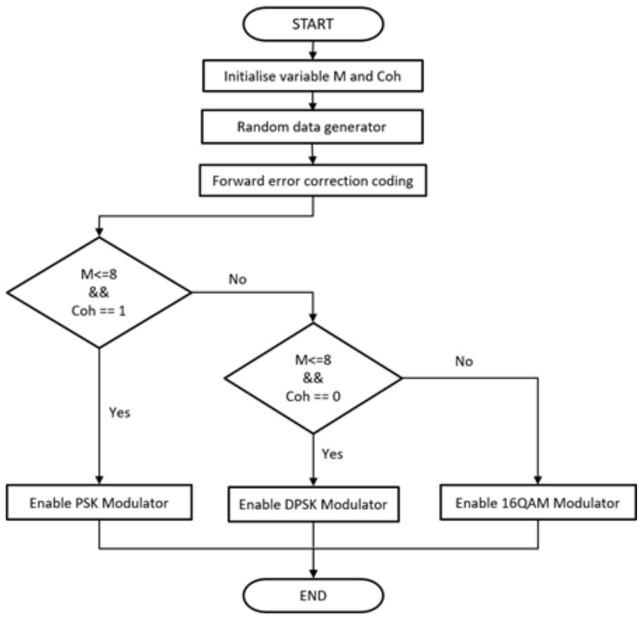

Fig.1. Flow chart of adaptive modulation scheme

In the convolutional encoder diagram defined in IEEE STD 1901.2 [5], has six memory elements and one current input bit. Therefore, the constraint length is seven and code rate is ½. The binary representation is obtained by assuming 1 in the place where a tap connection feeds the modulo two adder and 0 elsewhere.

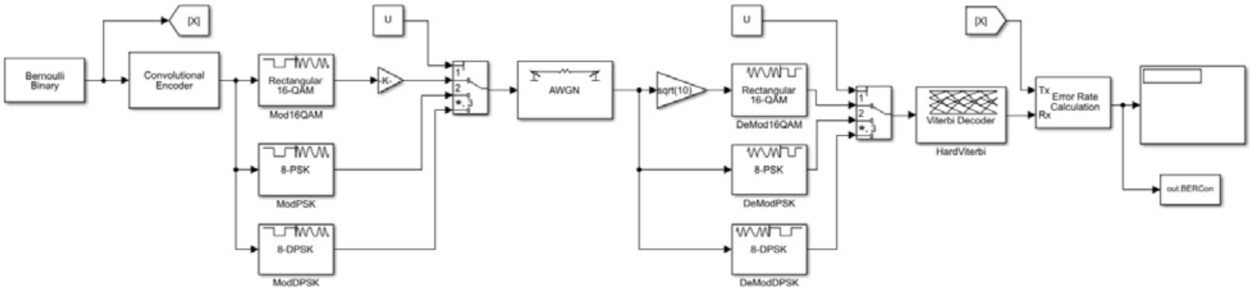

Fig.2. Model of Viterbi decoded convolutional coding with the adaptive modulation scheme

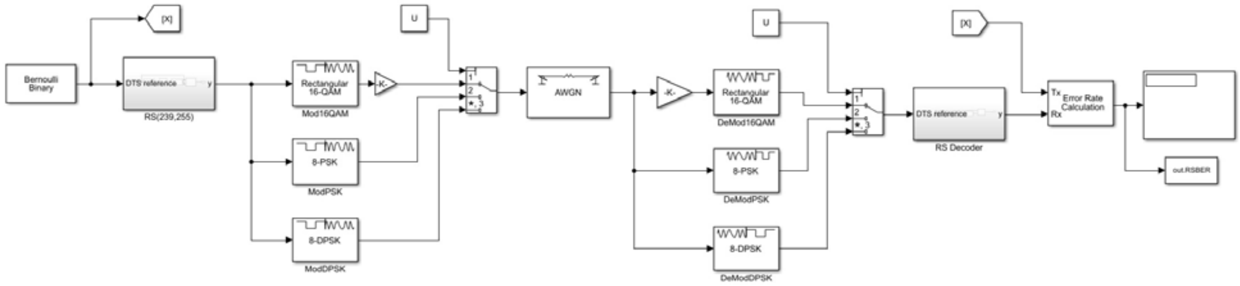

Fig.3. Model of binary input Reed-Solomon coding with the adaptive modulation scheme

The oldest input occupies the right most position and the leftmost one is the present input bit to the encoder. Thus, the first output is defined by binary 1111001 and its octal equivalent is 171.

The second output is defined by tap connection 1011011 in a binary form whose octal equivalent is 133. A trellis structure describes how the state transition occurs to the input of the encoder to obtain the first and the second output of the convolutional encoder. Using Matlab function poly2trellis, the constraint length and two output octal pairs are converted to a valid trellis structure. The normalization factor for 16QAM as per IEEE STD 1901.2 [5] to achieve the same average power for all the mapping is implemented in the model. The mapping constellation defined in the standard [5] is implemented in the model through Matlab code.

At the receiver end, the demodulator demodulates the received data and feeds the Viterbi decoder. In the Viterbi decoder, the conversion of symbols to original data is accomplished by tracing the most accurate path backward through the trellis. The decoder sends out the decision on a bit after several iterations to find the most accurate path, the number of trellis state processed is referred to as traceback depth. The convolutional encoder used in the model is non-punctured and traceback length recommended is 6 to 7 times the constraint length. Most hardware implementation requires this parameter to be multiple of 6 [8] and hence in the model the traceback length is taken as 48. The convolutional encoder is initialized to binary 0000000 at the beginning, the decoder sends out zero symbols before the actual first encoded bit reaches the decoder output. To account for this delay, the delay parameter in the error is set to a value equal to traceback depth.

The simulation result is verified against the theoretical upper bound bit error probability (P_b) using equation 1 to 3 [9]

(1) $$P_b < \sum_{d=d_{free}}^{\infty} a_d f(d) P_2(d)$$

where: d_{free} – free distance, $P_2(d)$ – Pairwise error probability, a_d – the number of paths of distance d, f(d) - exponent of state variable N.

For odd value of d,

(2) $$P_2(d) = \sum_{k=\frac{d}{2}+1}^{d} \binom{d}{k} p^k (1-p)^{d-k}$$

where: p – bit error rate of uncoded channel.

And when d is even,

(3)

$$P_2(d) = \sum_{k=\frac{d}{2}+1}^{d} \binom{d}{k} p^k (1-p)^{d-k} + \frac{1}{2}\binom{d}{\frac{d}{2}} p^{\frac{d}{2}} (1-p)^{\frac{d}{2}}$$

Reed-Solomon coding model design

In this article, performance of RS encoder with codeword length (N_{rs}) of 255 and message length (K_{rs}) 239 in normal mode as specified in IEEE STD 1901.2 is analysed.

The model configuration illustrated in figure 3 is same as the convolutional encoder. According to IEEE standard, the first bit in time from data scrambler is the MSB of integer input of RS encoder. The sample frame size parameter of random binary generator is set to value equal to K_{rs} times M_{rs}. The bit stream from generator is converted to integer so as to have block of 239 bytes input message to RS encoder. The output of RS encoder, proceeds in time with MSB of first message byte first followed by parity.

The primitive polynomial is set as [1 0 0 0 1 1 1 0 1] in RS encoder block to meet the requirement of IEEE STD 1901.2 [5],

(4) $$\alpha^1 = x^8 + x^4 + x^3 + x^2 + 1$$

where: α - primitive component in Galois Field (GF – 2^8).

RS encoder being a type block codes, transmits data in blocks of symbols. For every K_{rs} encoder input message, parity-check symbols are added to produce a total of N_{rs} symbols to transmit. The code rate is K_{rs} / N_{rs}.

The code word length N_{rs} and message length is given by equation 5 and 6,

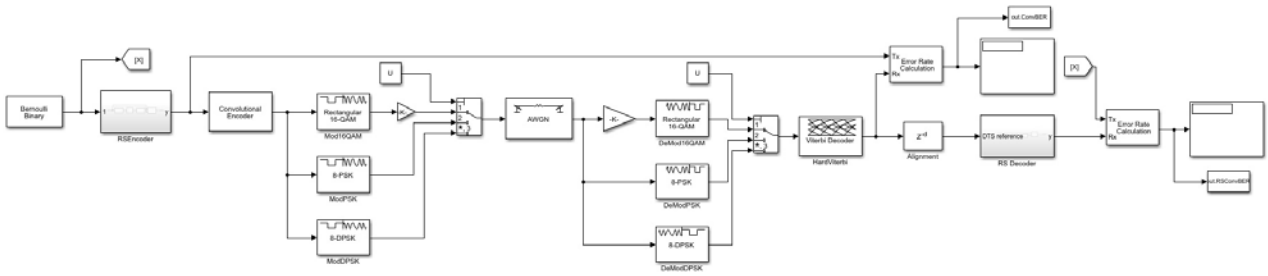

Fig.4. Model of Concatenated Reed-Solomon – Convolutional coding with the adaptive modulation scheme

(5) $$N_{rs} = 2^{M_{rs}} - 1$$

where: M_{rs}– number of bits in one output symbol.

(6) $$K_{rs} = 2^{M_{rs}} - 1 - 2E$$

where: E– maximum number of errors that could be corrected.

Since there are $\binom{N_{rs}}{i}$ different ways of having i errors in N_{rs} symbols, the formula for probability of symbol error is [9],

(7) $$P_{Sym} = \frac{1}{N_{rs}} \sum_{i=E+1}^{N_{rs}} \beta_i \binom{N_{rs}}{i} p^i (1-p)^{N_{rs}-i}$$

where: β_i - is the average of symbol errors that remains in received data stream such that channel induces i symbol errors.

The bit error probability is related to symbol error probability as [9],

(8) $$P_b = \frac{2^{M_{rs}-1}}{2^{M_{rs}} - 1} . P_{Sym}$$

Concatenated coding model design

The interaction between the two main coding schemes in IEEE STD 1901.2, i.e., Reed-Solomon and Convolutional code is investigated by the model shown in figure 4. The channel of RS encoder consists of inner Viterbi-decoded convolutional encoder and AWGN channel, thus the inner decoder reduces the number of errors seen by the outer decoder. The error which is failed to detect by the inner coding (convolutional) is detected and corrected by outer RS coding. A high-rate outer code is desirable to be immune against burst noise and RS coding is used for this purpose. RS code performance depends on the symbol errors in the block and is immune to burst errors of length up to Mrs times E bits. The total code rate (R_{tot}) is equal to the rate of the inner convolutional code times the rate of the outer Reed- Solomon code.

(9) $$R_{tot} = \frac{1}{2} . \frac{K_{rs}}{N_{rs}}$$

The probability of error of the concatenated code is obtained by simulating symbol error probability of inner Viterbi decoder (P_V) for inner E_b/N_o and applying it to the outer coding for total E_b/N_o.

(10) $$EbNo_{tot} = EbNo_{inner} . \frac{1}{R_{out}}$$

where: R_{out} - rate of outer RS code.

The theoretical upper bound of the concatenated model is obtained from equation (7) as,

(11) $$P_b = \frac{1}{N_{rs}} \sum_{i=E+1}^{N_{rs}} (i+E) \binom{N_{rs}}{i} P_v^{\,i} (1-P_v)^{N_{rs}-i}$$

where: P_V- symbol error probability of inner Viterbi decoder, E - maximum number of error symbol that could be corrected by RS outer code.

The delay equals to the traceback depth caused by inner Viterbi decoder is aligned to the input frame size of RS decoder using delay block. This is required for proper bit error rate calculation as the RS decoder take block of 255-byte data for processing. The BER performance of concatenated coding is evaluated for all mapping schemes listed in IEEE STD 1901.2.

Simulation model results

The objective of the simulation in this article is to evaluate the BER performance of individual RS code and Viterbi decoded convolutional code in comparison with the BER performance of concatenated RS – Convolutional code. At the receiver end, BER is evaluated using error calculation block for varying E_b/N_o and the output is transferred to workspace variable of Matlab for plotting the BER curve. Figure 5, 6 and 7 shows the BER performance of RS code, Viterbi decoded convolutional code and concatenated Reed-Solomon – Convolutional code respectively obtained from simulation for all mapping schemes listed in IEEE 1901.2 standard.

In figure 8, BER performance of concatenated Reed-Solomon – Convolutional code is compared to individual coding performance for three types of mapping. From simulation results, it is evident that most of the random errors perceived at the decoder is able to correct by convolutional code, but is not immune to burst error.

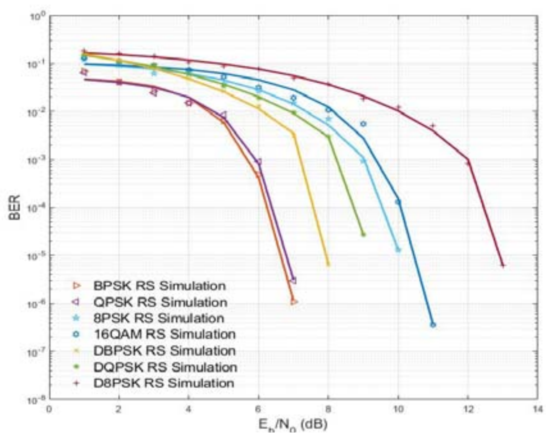

Fig.5. BER plot of RS code.

RS code has tremendous advantage over burst error. In the case of (255,239) RS code, each symbol has 8 bits (one byte) and the code can fix up to 8 symbol errors. Now assume the presence of burst error in the channel of continues 40 bits of duration in one block (255 symbols) of data being transmitted. At RS decoder, it replaces corrupted symbol with correct byte of information and is capable of correcting 8 symbols (64 bits) in one block of data, thus burst error of 40 bits could be easily fixed by RS decoder.

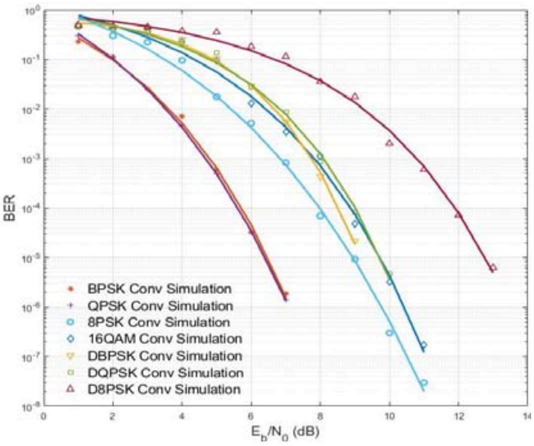

Fig.6. BER plot of Viterbi decoded convolutional code.

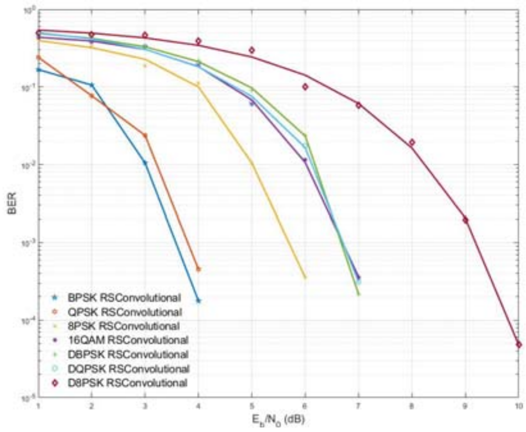

Fig.7. BER plot of concatenated RS – Convolutional code.

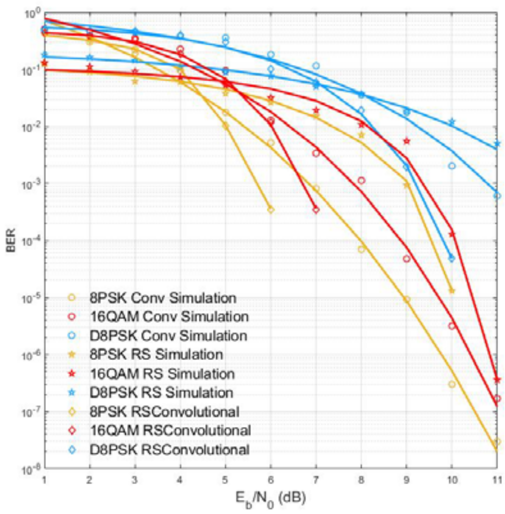

Fig.8. Comparison of RS code, Convolutional code and the concatenated code.

Conclusion

Theoretical and analytical analysis of three error correcting codes RS code, Viterbi decoded convolutional code and RS – Convolutional code were presented in this article. With the concatenated code, a portion of random errors in the channel is addressed by the inner Viterbi decoded convolutional code. The random errors beyond the error correction capability of the inner code and burst errors of length within 8 symbols is fixed by the outer RS code. Thus, the concatenated RS – Convolutional code is effective for combined random-burst channel errors. Moreover, it offers easy implementation at low cost. An interleaver may be added at the output of inner code to further improve the performance. Therefore, concatenated code is best suited for PLCC.

***Authors**: Chandralekha Mohanachandran, Research Scholar, RNS Institute of Technology, Bengaluru, India, E-mail: chandralekha85@gmail.com; Dr Srinivasan Sumathi, Professor and Head of Electrical and Electronics Engineering Department, RNS Institute of Technology, Bengaluru, India, E-mail:sumathisrinivasan1@gmail.com.*

REFERENCES

[1] G. Prasad, Y. Huo, L. Lampe, A. Mengi and V. C. M. Leung, "Fault Diagnostics with Legacy Power Line Modems," 2019 IEEE International Symposium on Power Line Communications and its Applications (ISPLC), Praha, Czech Republic, 2019, pp. 1-6, doi: 10.1109/ISPLC.2019.8693385.

[2] R. R. Mohassel, A. S. Fung, F. Mohammadi and K. Raahemifar, "A survey on advanced metering infrastructure and its application in Smart Grids," 2014 IEEE 27th Canadian Conference on Electrical and Computer Engineering (CCECE), Toronto, ON, 2014, pp. 1-8, doi: 10.1109/CCECE.2014.6901102.

[3] A. Al-Mulla, A. ElSherbini, Demand management through centralized control system using power line communication for existing buildings, Energy Conversion and Management, Volume 79, 2014, Pages 477-486, ISSN 0196-8904, https://doi.org/10.1016/j.enconman.2013.12.011

[4] Chandralekha M and Sumathi S (2021). A Survey on Narrow Band Power Line Carrier Communication for Efficient and Secure Data Transmission in Smart Grid Applications, I3CAC EAI. DOI: 10.4108/eai.7-6-2021.2308770.

[5] Institute of Electrical and Electronics Engineers, Power Line Communications Standards Committee. IEEE Std 1901.2: IEEE Standard for Low-Frequency (less than 500 kHz) Narrowband Power Line Communications for Smart Grid Applications, 1st ed.; 3 Park Avenue, NY, October 2013.[Revised Sept. 2015]

[6] C. Mohanachandran, "Simulation of Mapping Schemes as Per STD IEEE1901.2 for Power Line Carrier Communication," 2021 International Conference on Circuits, Controls and Communications (CCUBE), 2021, pp. 1-6, doi: 10.1109/CCUBE53681.2021.9702718.

[7] Remigius O. Okeke and Ifeoma B. Asianuba (2019). Performance Evaluation of WiMAX Physical Layer Using Matlab Simulink. American Journal of Engineering Research (AJER). Volume-8, Issue-6, pp-34-43. e-ISSN: 2320-0847 p-ISSN : 2320-0936.

[8] AMD XILINK, "Vivado Design SuiteViterbi Decoder v9.1," PG027Product Guide, February 4, 2021.

[9] John G. Proakis and Masoud Salehi, Digital Communications, 5th ed. New York: McGraw-Hill, 2008.