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Development of single-phase single switch AC-DC Zeta converter for improved power quality

***Abstract**. A new topology of single–phase single switch non-isolated AC-DC Zeta converter is presented in this paper. The proposed topology in open loop operation can provide high conversion efficiency under duty cycle variation. Proposed converter with feedback controller provides high input power factor of 0.99 and reduced input THD while maintaining 900V DC output voltage. The converter exhibits stable dynamic response for sudden load change. Analysis and simulation results of the circuit are obtained using software simulation.*

***Streszczenie.** W artykule przedstawiono nową topologię jednofazowego, jednoprzełącznikowego nieizolowanego przekształtnika AC-DC Zeta. Proponowana topologia w pracy w otwartej pętli może zapewnić wysoką wydajność konwersji przy zmianach cyklu pracy. Proponowany przekształtnik z kontrolerem sprzężenia zwrotnego zapewnia wysoki współczynnik mocy wejściowej 0,99 i zmniejszone THD wejściowe przy zachowaniu napięcia wyjściowego 900 V DC. Przetwornik wykazuje stabilną dynamiczną odpowiedź na nagłą zmianę obciążenia. (**Opracowanie jednofazowego przetwornika AC-DC Zeta w celu poprawy jakości energii**)*

Keywords: Zeta converter, AC-DC power conversion, Power factor correction controller, Buck-Boost converter
Słowa kluczowe: in the case of foreign Authors in this line the Editor inserts Polish translation of keywords.

Introduction

AC-DC converters with step-up and step-down topologies have been utilized in numerous sectors. Apart from it's use in residential, commercial and industrial fields; it has now been used in transportation and different utility systems. Advanced application like battery chargers for electric vehicles now require the service of AC-DC converters. As the sources of fossil fuels are diminishing rapidly, people are now focusing more on renewable energy resources to mitigate the energy crisis. Renewable energy resources including grid connected solar photovoltaic energy conversion systems and wind energy conversion system require the extensive use of AC-DC converters [1].

Traditionally, full wave rectifier with bridge configuration is used for AC-DC power conversion that has the property of simple structure and low cost. However, these rectifiers have some drawbacks that includes pulsating input current, high electromagnetic interference (EMI), low input power factor, harmonic pollution at power system and so on [2-3]. Harmonic pollution is detrimental to power supply that can cause malfunction or damage to sensitive electric devices. The harmonics present in power supply needs to be within a tolerable limit prescribed either by IEEE 519-1992 or IEC 61000-3-2/IEC 61000-3-4 standard [4]. Many methods have been proposed to mitigate harmonic pollution in the recent years. In general, input passive filters consisting of large inductor and capacitor are used to reduce harmonic distortion (THD) sacrificing performances like efficiency and power factor [5]. Again, use of bulky inductor and capacitor are not suitable for high power application. With a view to mollifying these problems switch mode converters have been proposed. These converters employ a DC-DC converter in between rectifier and load. The DC-DC converter use unidirectional switch for switching purpose, which may be a BJT, MOSFET or IGBT. There has been a deep study in switch mode power converters. These converters are classified as Buck, Boost and Buck-Boost for the basic topology. In these topologies a single inductor is used for circuit operation. There are also some higher order topologies like Cuk, SEPIC and Zeta in which two inductors are employed in the circuit. Several isolated and non-isolated topologies have also been introduced for different switch mode converters [3,6].

The Zeta converter, also known as Inverse SEPIC converter is a fourth order converter constructed using a switch, semiconductor diode, two capacitors and two inductors. A PWM feedback loop is needed to regulate output voltage that can be stepped up or down [7]. Zeta converter with high frequency transformer isolation can provide safety in the system but the topology has high transistor voltage stress because of resonance caused by HF transformer leakage inductance and capacitance of transistor switch. An isolated Zeta converter with two-transistor and two clamping diodes on primary side of transformer was proposed that is capable of reduce the transistor voltage stress [8]. Dual-Zeta converter proposed in [9] can reduce the output voltage ripple and share load as two converters work simultaneously but out of phase. A bridgeless Zeta converter with isolation proposed in [10] used interleaved topology to reduce diode losses and output ripple. Fuzzy Logic Controller was used for discontinuous mode operation for the converter. Authors in [11] proposed a Zeta converter for step down operation in electric vehicles application; wherein two stage conversion process and two PI controller was used. Transformer-less AC-DC Zeta converter was used for Permanent magnet synchronous motor using direct torque control technique [12]. Applications of Zeta converter was mainly low power applications with stepped down output voltage; i.e., Led driver [10], electric vehicle battery charger [11], PV applications [13] etc.

Transformer-less AC-DC Zeta topology with both Buck and Boost mode operation able to provide high power quality is the target of this paper. In this paper, a new single phase single switch non-isolated AC-DC Zeta converter is reported. The proposed converter can chop input current by using only one switch. This topology is different from conventional DC-DC regulated rectifiers because switching of input current ensures input AC current to be almost in phase with supply voltage without any additional control scheme. This would result in nearly sinusoidal input current shape with using of small EMI filter. This proposed converter can provide both step up and step down DC output voltage with high efficiency power conversion. Feedback controllers are also used to maintain certain voltage level with high input PF and low THD. Dynamic response of the proposed converter is also analyzed to verify converter response under different load switching.

Proposed Circuit Configuration

The proposed single-phase single switch AC-DC Zeta converter is shown in Figure 1. The proposed converter can provide non-inverting output voltage in both step up and step down modes. This topology has no isolation between source and load. There are five inductors (Lin, L1, L2, L3 and L4), five capacitors (Cin, C1, C2, C3 and C4), six diodes and a MOSFET switch (S1) in this topology. Input inductor (Lin) and capacitor (Cin) act as input filter for thiscircuit. C3 and C4 are output capacitor. Resistor R_0 is used as load.

a)

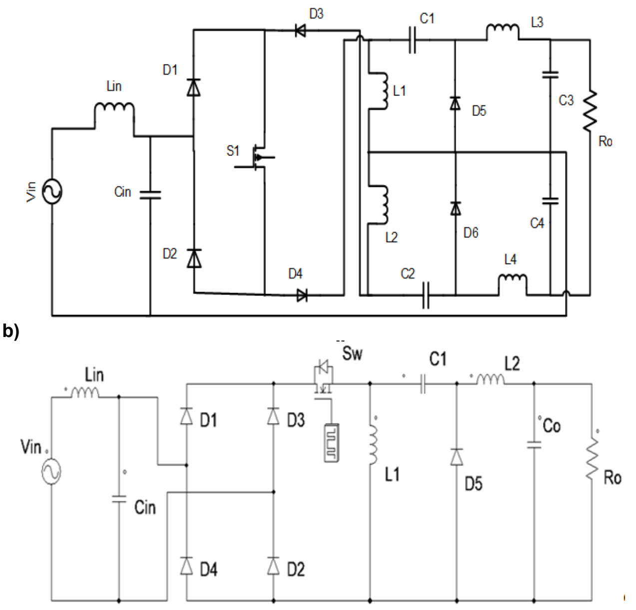

Fig.1. Proposed Single-Phase AC-DC Zeta Converter (a), Conventional Single-Phase AC-DC Zeta Converter (b)

Principle of Operation

The proposed AC-DC Zeta converter has four operating states – positive and negative half cycles each with switch ON and OFF condition.

Mode 1:
When S1 is on for positive half cycle, D1 and D4 is ON whereas D2 and D3 is OFF. Inductor L1 and L3 is charged. C2 and L2 creates a loop, and L4 and C4 also creates a loop as D6 is ON.
Mode 2:
When switch S1 is OFF for positive half cycle of input, Vin is isolated from the main circuit. C3 and C4 is charged by L3 and L4 respectively.
Mode 3:
When S1 is on for negative half cycle, diode D1 and D4 is OFF whereas D2 and D3 is ON. L3 and L4 is charged in this cycle.
Mode 4:
For negative cycle and S1 OFF condition, source is isolated from the main circuit. C3 and C4 is charged again by L3 and L4 respectively.

Ideal Voltage Gain Equation of the Proposed Converter

When switch S1 is ON, the voltage across inductor L1

(1) $v_{L1} = v_{in}$

When switch is OFF,

(2) $v_{L1} = v_{C1}$

v_{L1} and v_{C1} the the voltage of L1 and C1 respectively.
The volt-sec balance over a line frequency period will be zero. For full supply cycle of N switching per period,

(3) $$\sum_{n=1}^{N}\int_{t_i}^{t_i+T_{Sw}} v_{L1}dt = \sum_{n=1}^{N}\int_{t_i}^{t_i+DT_{Sw}} v_{in}dt + \sum_{n=1}^{N}\int_{t_i+DT_{sw}}^{t_i+T_{Sw}} v_{C1}dt = 0$$

Here, T_{sw} is switching time period, DT_{sw} is ON time period of switch and D is the duty ratio. Now, assume,

(4) $v_{in} = v_{in\max}\sin(\omega t - \theta_{in})$

(5) $v_{C1} = v_{C1\max}\sin(\omega t - \theta_{C1})$

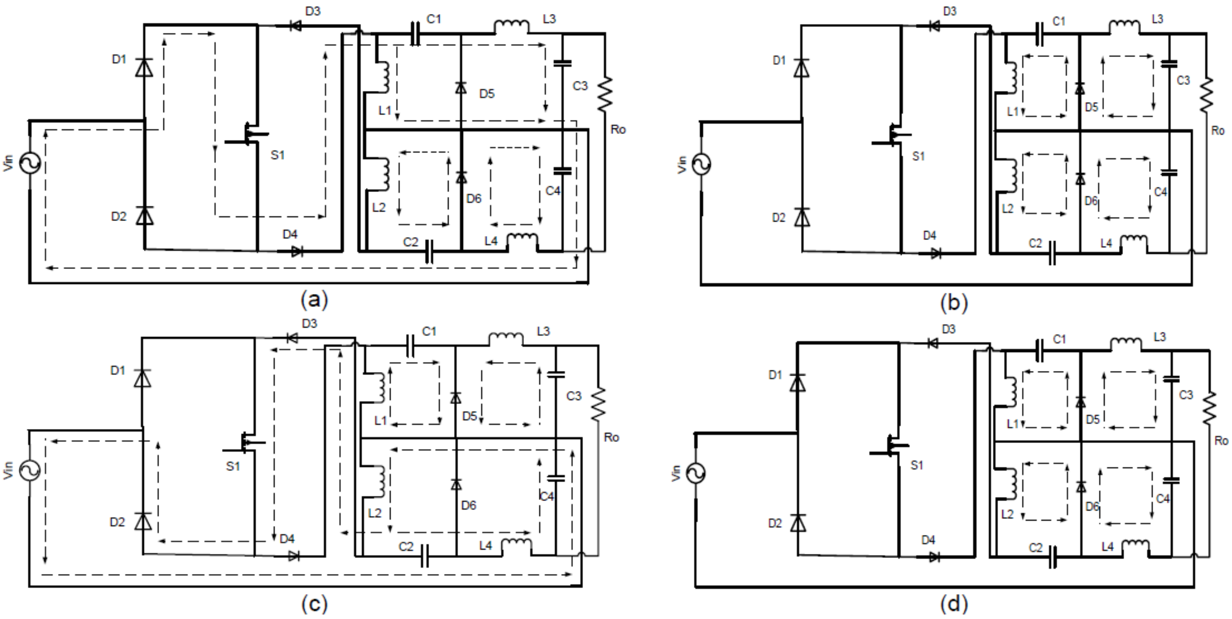

Fig. 2: Four Modes of Operation of Proposed AC-DC Zeta Converter (a) Mode 1:Proposed circuit in positive half cycle when S1 is ON.(b) Mode 2:Proposed circuit in positive half cycle when S1 is OFF. (c) Mode 3:Proposed circuit in negative half cycle when S1 is ON.(d)Mode 4:Proposed circuit in negative half cycle when S1 is OFF

From eqn (3), we get after integration,

(6) $$\sum_{n=1}^{N} v_{C1\max}\sin(\omega t_i-\theta_{C1}) = -\frac{D}{1-D}\times\sum_{n=1}^{N} v_{in\max}\sin(\omega t_i-\theta_{in})$$

Again at the output stage for inductor L3, when the switch S1 is ON,

(7) $$v_{L3} = v_{in} - v_{C1} - v_{C3}$$

when the switch is OFF,

(8) $$v_{L1} = -v_{C3}$$

Now the volt-sec balance for N cycle of line frequency can be expressed as

(9) $$\sum_{n=1}^{N}\int_{t_i}^{t_i+DT_{Sw}}(v_{in}-v_{C1}-v_{C3})dt = \sum_{n=1}^{N}\int_{t_i+DT_{sw}}^{t_i+T_{Sw}} v_{C3}dt$$

Putting the initial conditions and integrating for the total time period we obtain the following

(10) $$\sum_{n=1}^{N} v_{o\max}\sin(\omega t_i-\theta_o) = \frac{2D}{1-D}\sum_{n=1}^{N} v_{in\max}\sin(\omega t_i-\theta_{in})$$

Thus the average value of output voltage can be expressed as

(11) $$v_{oavg} = \frac{1}{\pi}\int_0^{\pi} v_{o\max}\sin\theta d\theta$$

(12) $$v_{oavg} = \frac{2D}{1-D}\times\frac{2v_{in\max}}{\pi}$$

Table 1: Voltage gain comparison under duty ratio variation

Duty cycle	Voltage Gain (Theoretical)	Voltage Gain (simulation)
0.1	0.20	0.25
0.2	0.45	0.57
0.3	0.77	0.95
0.4	1.20	1.33
0.5	1.80	1.63
0.6	2.70	2.05
0.7	4.21	2.66
0.8	7.21	3.38
0.9	16.22	4.68

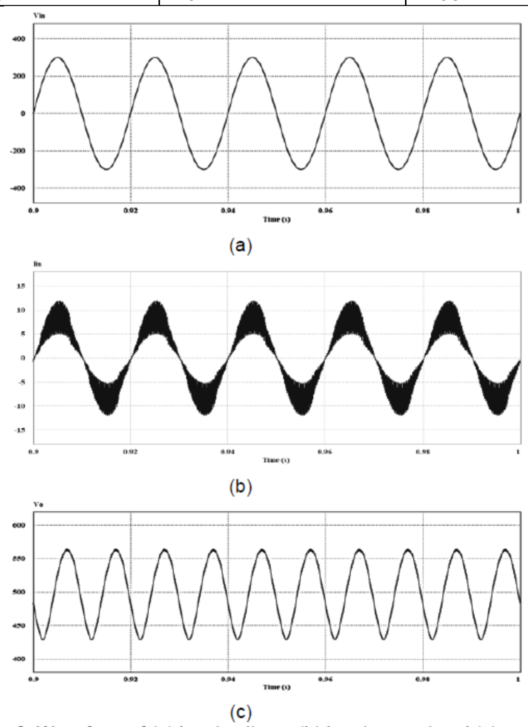

Fig 3. Waveform of (a) input voltage, (b) input current and (c) output voltage

The proposed converter can work in both step up and step down mode as seen from equation (12) . The ideal voltage gain is compared with simulated results and tabulated in Table 1. For high duty ratios, the difference between the theoretical and simulated results is higher. But for low duty ratios both the gains are comparable.

Simulation and Results

PSIM software is used for simulation of the proposed circuit configuration. For simulation of Zeta configuration 300V (peak) ac source with the frequency of 50 Hz is employed. MOSFET is selected as the switching device. The switching frequency is set at 5 kHz. Here, Inductor Lin and capacitor Cin form the input filter with corresponding values of Lin = 5mH and Cin = 1μF.The value of L1 and L2 is chosen as 4mH. C1 and C2 are chosen as 10μF and C3 and C4 have a value of 110μF. A resistor R_o of 100Ω is used as the load of the converter. Typical input voltage, input current and output voltage waveforms are shown in fig. 3 for the proposed single phase AC-DC Zeta converter.

Open loop analysis under duty cycle variation

The proposed converter is simulated for duty cycles 0.1 to 0.9 and tested with different performance parameters. The key converter performance parameters are conversion efficiency, input power factor and input current THD.

Table 2: Open loop analysis of proposed converter for different duty ratio

Duty cycle (D)	Efficiency (%)	Input current THD (%)	Input Power Factor	Voltage Gain
0.1	97.05	51.46	0.67	0.25
0.2	98.09	61.67	0.75	0.57
0.3	97.78	45.91	0.87	0.95
0.4	96.96	33.33	0.95	1.33
0.5	95.63	27.27	0.96	1.63
0.6	95.88	22.56	0.97	2.05
0.7	95.49	17.44	0.97	2.66
0.8	95.21	17.35	0.96	3.38
0.9	95.06	6.57	0.75	4.68

It is evident from the Table 2 that the proposed converter has efficiency range 95.06% to 98.09%. It has good efficiency for all duty cycles, which is a great attribute for a converter. Also it has good input PF except for some duty cycles. The proposed converter can give step down output up to 30% duty ratio and step up output for rest of the duty ratios. THD of input current decreased with the increase of duty cycles.

Table 3: Open loop analysis of proposed converter for load variation (D=0.7)

Load (Ω)	Efficiency (%)	Input Current THD (%)	Input Power Factor	Voltage Gain
50	95.71	19.23	0.97	1.72
100	95.49	17.44	0.97	2.66
150	93.66	17.82	0.96	3.22
200	93.53	18.35	0.96	3.70
250	93.25	18.76	0.96	4.10
300	93.09	19.22	0.96	4.46
350	92.72	19.51	0.96	4.79
400	92.64	19.82	0.96	5.11
450	92.13	20.09	0.96	5.40
500	92.14	20.28	0.96	5.70

Open loop analysis under load variation

For a fixed duty cycle, load is varied and performance parameters are tabulated in Table 3. Load is varied form 50Ω to 500Ω for duty cycle D=0.7.

It is seen form the Table 3 with the increase of load, the proposed converter is capable of providing good efficiency. As the load increases output voltage is increased, hence the gain of the proposed converter also increased. Input power factor remains almost same under load variation for the proposed converter.

Comparison of proposed converter with conventional converter under duty cycle variation

The proposed converter is compared with conventional Zeta converter in fig. 1(b) for duty cycle variation. Duty cycle is varied from 0.1 to 0.9 and performance of both converters is evaluated. The data used for conventional converter in fig. 1(b) are Lin = 5mH, Cin = 1μF, L1= 4mH, L2=4mH, C1= 10μF and Co= 220μF. The load is 100 ohm and switching frequency is 5 kHz for both the converters.

The proposed converter has better input power factor except for low duty ratios as illustrated in fig. 4.

The proposed converter has better efficiency for D=0.1 to D=0.6 than conventional converter as seen from fig. 5. At high ratios, the efficiency drops a bit lower than the conventional converters. The voltage gain of proposed topology is better for most instances of duty ratios than conventional topology as seen from fig. 6. The proposed converter is capable of providing more stepped up voltage as output than conventional one.

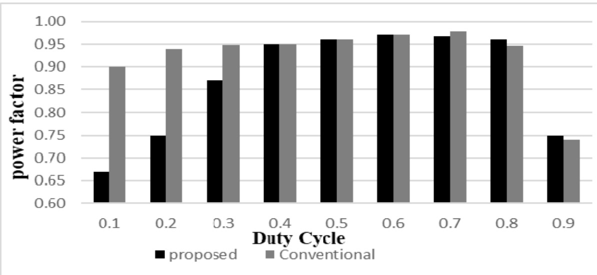

Fig. 4. Comaprison of input PF between proposed and conventional converter for duty cycle variation (Ro=100Ω, Fs=5 kHz)

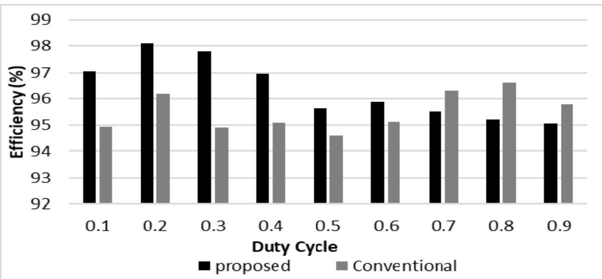

Fig. 5. Comaprison of efficiency between proposed & conventional converter for duty cycle variation (Ro=100Ω, Fs=5 kHz)

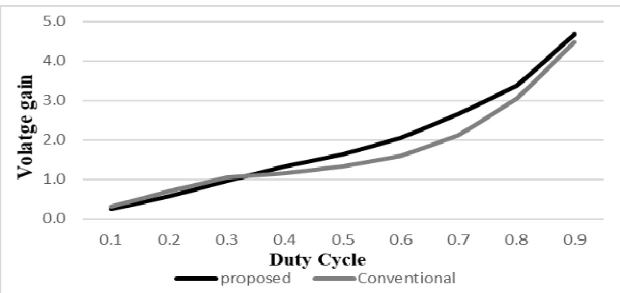

Fig. 6. Comaprison of voltage gain between proposed & conventional converter for duty cycle variation (Ro=100Ω, Fs=5kHz)

Comparison of proposed converter with conventional converter under load variation

The proposed converter topology is compared with conventional Zeta converter for different load variation. The switching frequency is set to 5 KHz and duty cycle is maintained at 50%. Load Ro is varied from 50Ω to 500Ω. The proposed topology has much better efficiency than conventional topology throughout the variation of load as shown in fig. 7. The total harmonic distortion (THD) of input current is lesser in case of proposed topology for all load conditions. It is edident from fig. 8 that the achievable voltage gain is better for proposed converter than conventional converter for different loads.

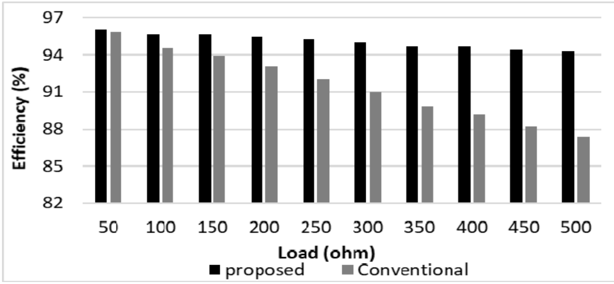

Fig. 7. Comaprison of efficiency between proposed and conventional converter for load variation (Fs=5 kHz, D=0.5)

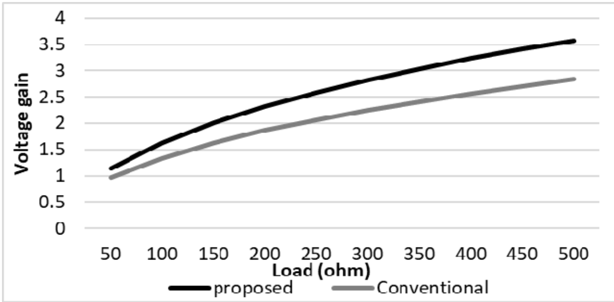

Fig. 8. Comaprison of volatge gain between proposed and conventional converter for load variation (Fs=5 kHz, D=0.5)

Comparison of proposed converter with conventional converter under switching frequency variation

The proposed converter topology is compared with conventional Zeta converter for different switching frequency variation. The load is taken as 100Ω and duty cycle is maintained at 50%. Switching frequency is varied from 5 kHz to 100 kHz. The proposed converter represents higher efficiency than the conventional converter throughout the variation of switching frequency. The proposed converter has better power factor than the conventional converter for mid to higher order of switching frequency.

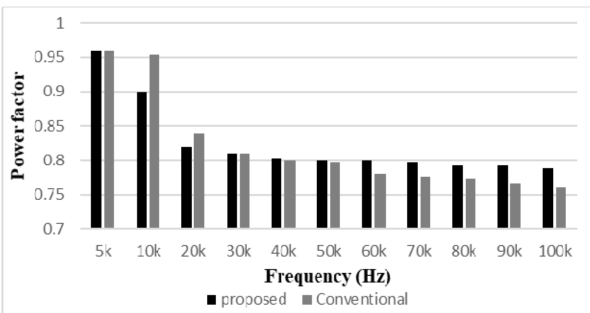

Fig. 9. Comparison of power factor between proposed & conventional converter under Fs variation (D=0.5 and Ro=100Ω)

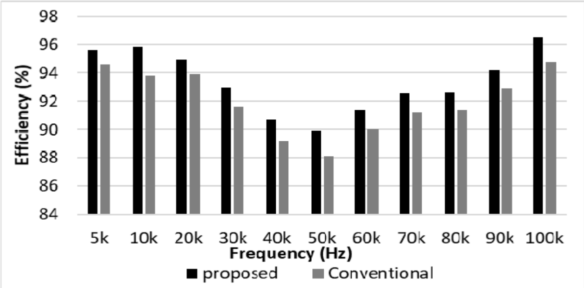

Fig. 10. Comparison of efficiency between proposed & conventional converter under Fs variation (D=0.5 and Ro=100Ω)

Proposed converter with PFC controller

Input PF of conventional AC-DC converters is relativley low in open loop mode of operation. Converters with efficiently designed Power Factor Correction (PFC) Controller can solve the problems due to low power factor. There are two loops in PFC controller, one is inner current loop and the other is outer voltage loop. The block diagram of a feedback controller of the proposed converter is illustrated in Fig. 11.

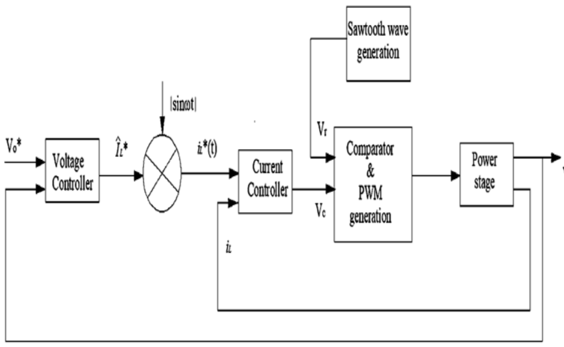

Fig. 11. Control loop for proposed feedback control system

The proposed converter used MOSFET as switch and it is PWM at constant frequency. The current i_L through the inductor have the form of full wave similar to Ivs(t)I as seen from Fig. 12, where $i_L = \bar{I}_L|\sin\omega t|$ and $|v_s|$ represents the absolute value of the supply voltage. The output voltage V_0 of the proposed converter can be greater or less than the peak of supply voltage $\hat{V}_s$ depending on duty ratio.

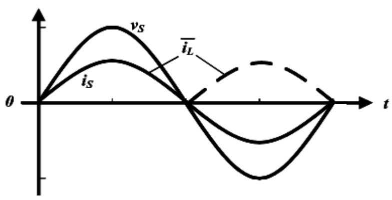

Fig. 12. PFC waveforms

The main target of the control scheme is to draw a sinusoidal current that should be in phase with the converter input voltage. The inductor current reference $i_L^*(t)$ has the full rectified form as shown in Fig. 12. The inner loop ensures the form of inductor current. The outer loop controls the amplitude of $i_L^*(t)$ based on V_o and maintains the output voltage at a fixed preselected value. When the current of inductor is not sufficient for any load, Vo will drop below reference voltage Vo*. The voltage of control system reshapes the amplitude of inductor current and thus Vo is maintained at its reference value. In this way voltage loop of controller maintains preselected output voltage for the converter. The error signal produced from reference and measured inductor current is fed to a current controller. Then the control voltage Vc(t) is taken from current controller. This voltage is compared with a ramp signal with peak voltage of Vr at switching frequency and switching signal d(t) is generated and then fed to MOSFET switch.

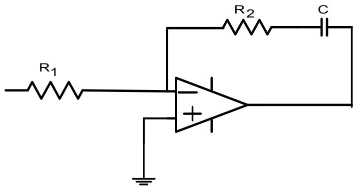

Fig.13. PI controller for feedback operation

The current and voltage control loop is designed using Proportional –Integral (PI) controller as seen in Fig. 13. The transfer function of PI controller is derived as

$$Hc(s) = -\frac{R_2}{R_1}\frac{(s+\frac{1}{R_2C})}{s} \quad (13)$$

Here, the PI controller is tuned with the values of R_1=10kΩ, R_2=220kΩ and C=0.022uF.

Simulation of the Proposed converter with designed controller

The feedback Controller is designed to maintain an average output voltage of 900V dc. From Fig. 14, it is edivdent that the input voltage and current are almost in phase and thus higher input power factor is achived for the proposed controller. The simulation results are tabulated in Table 4 in comparison with conventional converter and proposed converter without controller. With the addition of feedback controller, the proposed converter performed better in every area of performance parameters while maintaing desired voltage level.

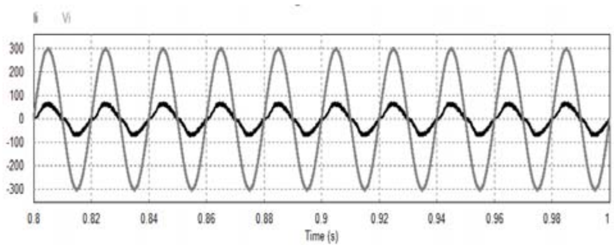

Fig. 14. Waveform of input current and input voltage for proposed converter with feedback controller

Table 4: Results of Simulation of the Converter with Feedback Controller (900V)

Performance Parameters	Conventional Zeta converter	Proposed converter Without Feedback	Proposed converter With Feedback
Efficiency (%)	90.63	92.34	92.94
Input PF	0.97	0.95	0.99
Input Current THD (%)	14.13	16.42	12.3

Dynamic response of Proposed converter with designed controller

Dynamic behavior response is a major design consideration for AC-DC converters. Many converters suffer from problems to maintain required voltage level under sudden change of load. Therefore, dynamic response is observed for AC-DC converters to maintain desired average output voltage. The proposed converter with feedback controller can achieve stable dynamic response for load variations. Reference voltage was set to 900 V with initial load of 200 Ω. Simulation was carried out for different load changes at different time as shown in Table 5. Fig. 15 illustrates the waveform of output voltage under dynamic load condition. It is observed that the proposed converter can maintain desired average output voltage of 900V dc.

Table 5: Load scheduling for dynamic response

Time (s)	Load(Ω)
0-0.5	200
0.5-0.8	66.6
0.8-1.2	100
1.2-1.5	150

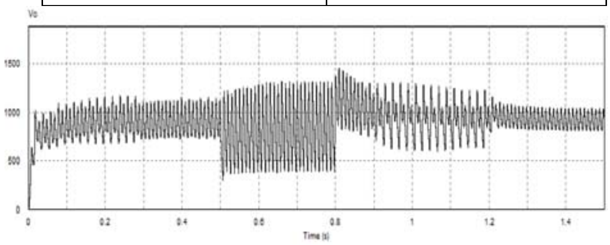

Fig. 15. Waveform of output voltage for dynamic response

Conclusion

It is evident from the open loop analysis that the proposed converter gives better conversion efficiency throughout the duty ratio variation than the conventional one. For lower and higher duty cycles, the proposed converter has some limitation in terms of input PF. This deficiency of input PF was overcome with the use of suitable closed loop controller which gives high input PF of 0.99. The closed loop controller gives higher efficiency even with high voltage gain than conventional converter. The proposed topology has high total harmonic distortion of input current in some of the duty cycle variations. Again, feedback controller solves this problem and the THD of input current was kept within the boundary. It can be said that the proposed converter has some deficiency in terms of input PF and input current THD for some of the duty ratio variation, but with the use of suitable feedback controller these shortcomings are corrected. The use of closed loop feedback controller not only provides higher conversion efficiency but also gives better input current THD and PF.

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