Fedor VASILYEV[1], Vladimir ISAEV[1], Maksim KOROBKOV[1]

Moscow Aviation Institute (National Research University) (1)

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The influence of the PCB design and the process of their manufacturing on the possibility of a defect-free production

Abstract. *The influence of the design parameters (width of the conductor, thickness of the copper foil and gap between the conductors) of the printed circuit board and the characteristics of the technological process of its production: stages of exposure and etching, on the output of defect-free products is considered. According to the results of the study, analytical dependences were obtained, which make it possible to determine the minimum width of the conductor depending on the thickness of the copper foil and etching factor. There is the model proposed that links the probability of manufacturing a defect-free printed circuit board with the parameters considered. The developed model can be extended with other design parameters and models of technological stages.*

Streszczenie. *W pracy dokonano oceny wpływu parametrów konstrukcyjnych płytki drukowanej (szerokości ścieżki, grubości folii miedzianej i szczeliny między ścieżkami) oraz charakterystyki procesu technologicznego jej wytwarzania: etapy naświetlania i trawienia, na wytwarzanie płytek PCB wolnych od wad. W ramach badań uzyskano zależności analityczne, które pozwalają określić minimalną szerokość ścieżki w zależności od grubości folii miedzianej oraz tzw. współczynnika trawienia. Zaproponowano model łączący prawdopodobieństwo wyprodukowania płytki drukowanej wolnej od defektów z rozważanymi w pracy parametrami. Opracowany model można rozszerzyć o inne parametry projektowe oraz modele etapów technologicznych podczas wytwarzania PCB. (**Wpływ projektu obwodu drukowanego i technologii na możliwość produkcji bez defektów**)*

Keywords: printed circuit board design parameters, process characteristics, exposure, etching, analytical model, defect-free production.
Słowa kluczowe: parametry projektu płytki drukowanej, charakterystyka procesu, ekspozycja, wytrawianie, produkcja bez defektów.

Introduction

Today, the vast majority of electronics uses printed circuit boards (PCB). Not least due to the development of digital technologies, including the concept of the "Internet of Things", the volume of electronic devices production is increasing, over time the number and density of interconnections have increased more and more. And with a decrease in the width of the conductors and the size of the gaps between them, the amount of defective products increases sharply, which entails an irrational use of resources and large economic losses. Taking into account this fact, the area in which the problems of reducing and preventing rejects in production is being investigated becomes more relevant.

Many articles are devoted to this topic [1, 2], which offer various models, methods and approaches to increase the percentage of the yield of suitable products at all stages of its production. For the same purposes, in all modern computer-aided design tools, there are separate subsystems in which the designer must specify the rules, thereby forcing him to impose restrictions on the subsequent technological process [3, 4]. All the obtained results do not answer to the question of if it will be possible to manufacture a device or not, they provide only recommendations related to a particular stage of the product life cycle without any connection with each other. Currently, two approaches are most often used to determine the feasibility of manufacturing PCB: the first relies on expert judgment, and the second relies on experimental data [5, 6].

Therefore, there is a need to create a theoretical basis that will determine the probability of manufacturing a defect-free PCB under various conditions. When developing a mathematical core, it is advisable to use a modular structure in which each separate block describes the influence of a separate factor. This approach has the following advantages: it is possible to assess the influence of individual components on the result, when studying the influence of new factors, they can be easily added, and, at the same time, insignificant parts can be discarded to increase the speed of calculations.

The main task of PCB is to create connections between components: electrical through conductors and mechanical through dielectric base. Therefore, first of all, it is necessary to research the influence of design parameters and technological processes on the quality of this task. The process of chemical creation of conductors was chosen as the starting point for the study, since it is widely used in modern production and finds its place in most processes for manufacturing PCB, from the subtractive to semi-additive and combined methods [7].

Theoretical Basis

We consider the cross section of a conductor. In most cases, when designing electronics, an idealized version is used as a conductor cross-section, i.e. rectangle. But in fact, the etching process is isotropic, which entails the appearance of cup-shaped defects [8] and, as a consequence, a change in the width of the conductor throughout its thickness (Figure 1), which is usually characterized by an increase in the width of the conductor as it approaches the dielectric base (or to the bottom of the conductor).

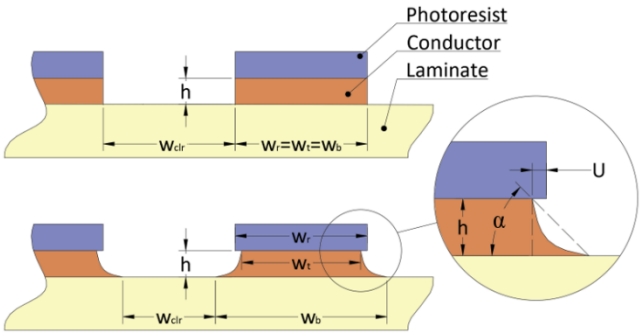


Fig.1. Parameters of ideal (top) and real (bottom) conductors: w_r– width of the photoresist covering the conductor; w_t– conductor top width; w_b– conductor bottom width; w_{clr} – gap between conductors, h – conductor thickness; U – underetching amount

To determine the effect of the etching process on the cross-section of the conductor, two characteristics are used: underetching *U* (1) and etching factor *F* (2), which characterize the average sagging of the photoresist and the average narrowing of the conductor per unit thickness, respectively [9].

(1) $$U = \frac{w_r - w_t}{2}$$

(2) $$F = \frac{2*h}{w_b - w_t} = tg(\alpha)$$

In the formulas (1) and (2): U is the underetching value [mm]; w_r is the photoresist width over conductor [mm]; w_t is the conductor top width [mm]; w_b is the conductor bottom width [mm]; F is the etching factor;
h is the conductor thickness [mm].

To determine the cross-sectional area of a real conductor (Figure 2), we need to know the law of change in the thickness of the conductor, depending on its width $\delta_h(x)$.

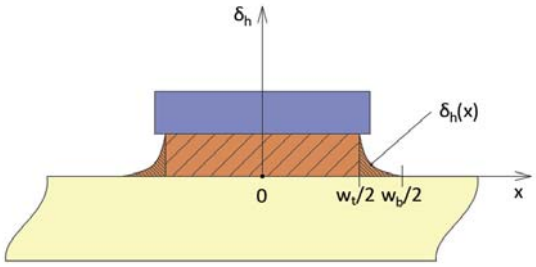
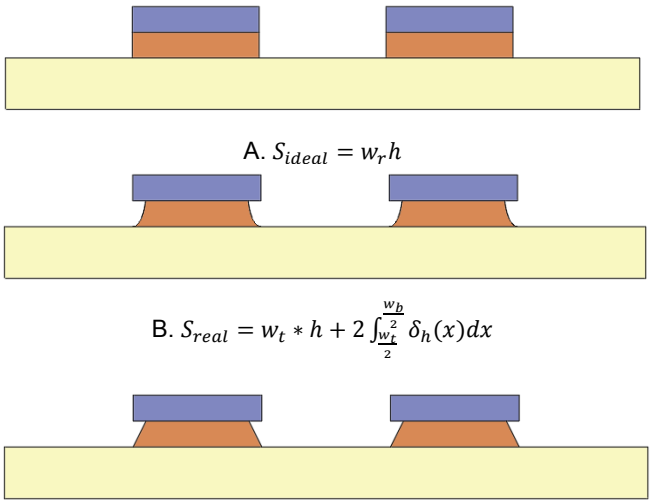


Fig.2. Determination of the cross-sectional area for real conductor

Taking into account the complexity of the geometry of the real conductor profile, which, depends on the technological process, it is advisable to approximate its edges by a straight line, thereby obtaining an isosceles trapezoid (Figure 3).

The described geometry of the conductor is only a special case, and an actual shape of the conductor depends mainly on the type of etching process and the installation in which the process takes place. For example, in high pressure jet etching plants, instead of tapering towards the top of the conductor, decrease in the center width is observed. When determining the parameters of the trapezoid, we can take the maximum width of the conductor as one base, and the minimum as the other.



A. $S_{ideal} = w_r h$

B. $S_{real} = w_t * h + 2\int_{\frac{w_t}{2}}^{\frac{w_b}{2}} \delta_h(x)dx$

C. $S_{model} = \frac{w_t + w_b}{2} h$

Fig.3. Determination of the cross-sectional area of conductor depending on its type (A - ideal case, B - real case, C - simplified case)

By combining formulas (1) and (2), it is possible to obtain the dependence of the cross-sectional area on the width of the photoresist covering the conductor, conductor thickness and parameters of the etching process (3).

(3) $$S_{model}(w_r, h, U, F) = \frac{w_t + w_b}{2} * h = w_r * h - 2U * h + \frac{h^2}{F}$$

Effect of the etching process on the conductors of PCB

The etching process is considered optimal if the etching value parameter, which is the ratio of the photoresist width to the width of the lower part of the conductor, is equal to one $\left(\frac{w_r}{w_b} = 1\right)$, since in this case the values for the maximum conductor width (bottom width) and the gap between the conductors correspond to the expected values. But, due to a possible change in the parameters of the technological process over time (an increase in the concentration of copper in the solution), during production, the appearance of underetching and overetching conductors is possible (Figure 4).

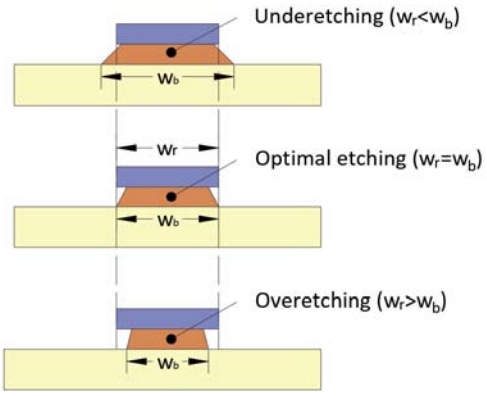


Fig.4. Image of the types of conductors in terms of etching

It should be noted that in production, obtaining overetching conductors is preferable to underetching ones, since it is preferable to preserve the gap value laid down at the design stage to prevent short circuits. Therefore, an increase in the width of the photoresist over the conductors w_r cannot be considered as a method to reduce the effect of the etching process, as this will reduce the gap. At present, in the production process, overetching is taken into account in the range of 10 - 15%.

The values of the underetching *U* and the etching factor *F* were obtained for a specific technological process of etching workpieces with a copper thickness of 35 μm in cupric chloride solution, which formed the basis for modeling and are necessary to determine the geometric parameters of the conductor (Table 1) [9].

Table.1. Technological process parameters

Etching time [s]	U [μm]	F	w_t [μm]	w_b [μm]
90	1.3	0.9	72.5	150.3
110	7.5	1.75	60	100
125	11	2.33	52.5	82.5
140	13	2.67	48.8	75
165	19	3.11	37.5	60

Next, we will consider the case of obtaining the optimal conductor $(w_r = w_b)$. Then, to find the cross-sectional area, it is enough to know only one parameter: underetching value *U* or etching factor *F*. Subsequently, from the selected parameter, it is possible to determine the upper base of the trapezoid. Using the etching factor *F*, the formula for determining the area is converted to the form (4).

(4) $$S_{model}(w_r, h, F) = \frac{w_t + w_b}{2} * h = \left(w_r - \frac{h}{F}\right) * h$$

According to the IPC-6012B standard [10], the reduction in the cross-sectional area of the conductor should not exceed 20% for electronic products with a high level of reliability (products of the third class according to IPC-A-600G [11]), therefore the following quality function of the etching process Q can be introduced (5).

(5) $$Q(w_r, h, F) = \frac{S_{model}(w_r,h,F)}{S_{ideal}(w_r,h)} * 100\%$$

If $Q > 80\%$, the conductor can be considered good, otherwise the conductor is defective. Also, this ratio allows obtaining the minimum width of the conductor that can be manufactured without defect using a specific etching process. An example of this calculation is shown in the Figure 5.

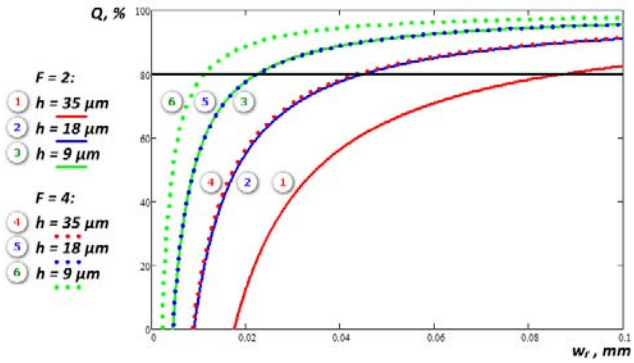


Fig.5. Dependence of the quality function *Q* on the width of the photoresist covering the conductor for different values of the foil thickness and etching factor

From the constructed family of curves of the quality function *Q* (5) versus the width of the photoresist covering the conductor, it can be concluded that an increase in the etching factor *F* by *n* times is equivalent to a decrease in the foil thickness *h* by *n* times (curves 2 and 4 or 3 and 5, Figure 5).

To determine the minimum track width, w_{min} can be made without defects, we use the following condition: $S_{model}(w_{min}, h, F) = 0.8 * S_{ideal}(w_{min}, h)$. Then the function of the minimum possible width will have the following form (6):

(6) $$w_{min} = 5 * \frac{h}{F}$$

Based on the obtained expression, it is easy to analytically prove the above judgment about the ratio of the etching factor and the foil thickness: for this, it is necessary to consider two technological processes (1 and 2) that provide the same minimum conductor width w_{min} with different etching factors (7).

(7) $$w_{min} = 5 * \frac{h_1}{F_1};\ w_{min} = 5 * \frac{h_2}{F_2} \Rightarrow \frac{h_1}{h_2} = \frac{F_1}{F_2}.$$

We build graphs of the dependence of the minimum conductor width on the foil thickness and etching factor (Figure 6).

The obtained results can be used only for an approximate assessment of the possibility of manufacturing PCB with a given width of conductors, since the resulting model does not take into account errors arise during the manufacturing process. Therefore, there is a need to transform the resulting model, and since changes in the geometry of the conductors are considered as defects, further consideration will be limited to the processes of formation of conductors, namely, exposure and etching ones.

Probabilistic model of exposure process

The quality of the layout obtained after the etching process is also influenced by the previous stage of exposure. The accuracy of the pattern reproduction at this stage depends on the production technology (contact, with microgap, projection, direct laser), photoresist parameters and on the resolution of the photomask, if it is necessary in the technological process.

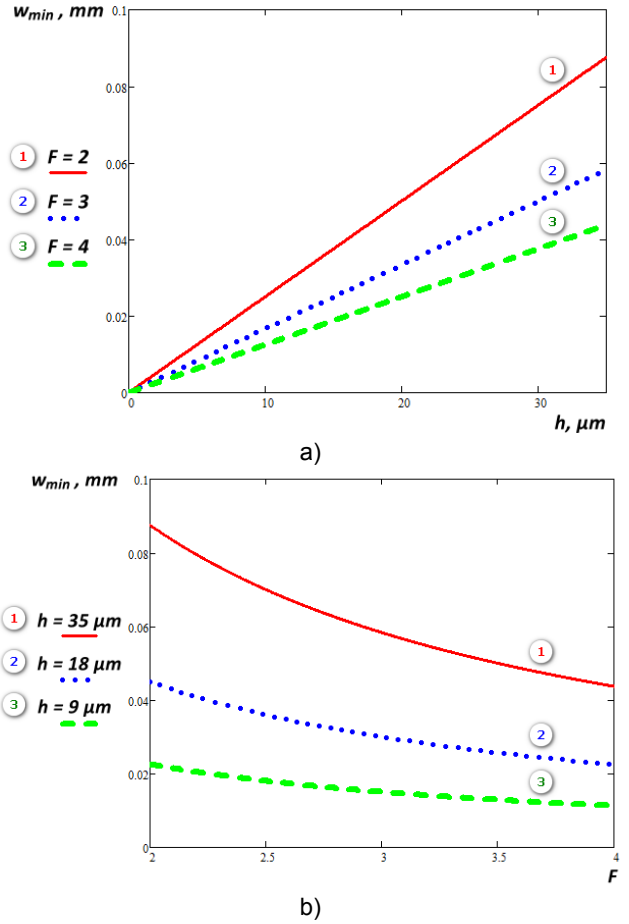


Fig.6. Graphs of the dependence of minimum possible width of the conductor on: a) thickness of the copper foil; b) etching factor

Each of the exposure technologies has its own advantages and disadvantages. Contact technology allows the most accurate reproduction of the pattern on the workpiece, but it has a large number of disadvantages associated with the use of photomasks: dependence of the accuracy of the topology on the resolution of the photomask, accuracy of its alignment, its material and its mechanical wear. Exposure with a microgap reduces the wear of the photomask, reducing the accuracy of the process, while retaining the remaining disadvantages of the contact method. Projection exposure is characterized by a large distance between the workpiece and the photomask, which makes it possible to minimize the wear of the latter, but the method requires expensive equipment, including a complex optical system. In modern production, laser direct exposure installations are popular, since in the production process there is no need to make a photomask and it is much easier to deal with misalignment of the pattern and the workpiece. The distribution of radiation intensity for various exposure technologies is shown in the Figure 7. It should be noted that the distribution of radiation intensity for direct laser technology has a similar appearance to projection exposure.

As a parameter characterizing the exposure process, we choose the roughness of conductor edge (ξ_{exp}). When creating a model, a direct laser exposure setup will be considered, in which the edge roughness parameter is ±10 μm.

We determine the distribution law that will describe the change in the width of the photoresist above the conductor after the exposure process. Since the exposure process is influenced by a large number of unrelated factors, then, according to the central limit theorem, it can be assumed

that the deviation of the conductor width from the ideal will obey the normal distribution law (8) with the probability density function (9).

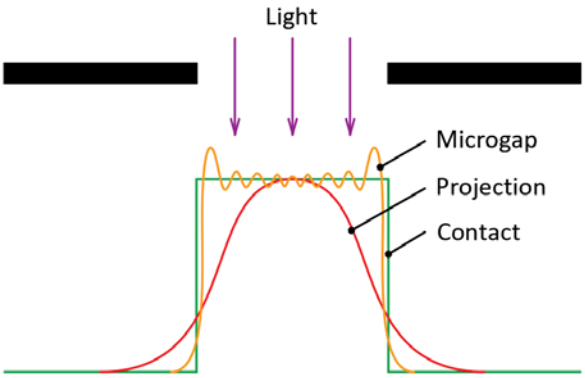


Fig.7. Radiation intensity distributions for different exposure technologies

To determine the normal distribution law, we only need to know the mathematical expectation and variance (or standard deviation). The mathematical expectation will be 0 $(M_{exp\_edge} = 0)$. Irregularity in the playback of the edge ξ_{exp}, in turn defines the interval $(M_{exp\_edge} - \xi_{exp}; M_{exp\_edge} + \xi_{exp})$, in which the edge of the conductor can change. It can be assumed that the length of this interval is $6\sigma_{exp\_edge}$, then the standard deviation will take the following form: $\sigma_{exp\_edge} = \frac{|\xi_{exp}|}{6}$.

(8) $$N_{exp\_edge} \in N\left(M_{exp\_edge}, \sigma_{exp\_edge}\right) = N\left(0, \frac{|\xi_{exp}|}{6}\right).$$

(9) $$f_{exp\_edge}(\Delta w) = \frac{1}{\sigma_{exp\_edge}\sqrt{2\pi}} exp\left\{-\frac{(\Delta w - M_{exp\_edge})^2}{2{\sigma_{exp\_edge}}^2}\right\}.$$

Also, we should not forget about the fact that when creating a wire, the exposure process affects its ends. Therefore, it is necessary to consider the composition of distributions to determine the resulting distribution law (10), in which the mathematical expectation and variance will be equal to the sums of the mathematical expectations and variances of its components, respectively.\

(10) $$N_{exp} = N_{exp\_edge} + N_{exp\_edge}.$$

Taking into account all above-mentioned, the mathematical expectation will remain equal to zero, and the standard deviation will take the following form: $\sigma_{exp} = \sqrt{2} * \sigma_{exp\_edge} = \frac{\sqrt{2}*\xi_{exp}}{6}$. Thus, the change in the width of the conductor is subject to the normal distribution law, given by the formula (11).

(11) $$N_{exp} \in N\left(0, \frac{\sqrt{2}*\xi_{exp}}{6}\right).$$

Mathematical model for the production of defect-free PCB

Similarly to the exposure process, we describe the effect of the etching process on the width of the conductor. This process will also be subject to the normal distribution law (12), but with different characteristics. Since the optimal etching process is considered, the mathematical expectation is equal to the width of the bottom of the conductor and the width of the photoresist $(M_{etch} = w_b = w_r)$. Standard deviation σ_{etch} will vary depending on the type of etching installation, solution and thickness of copper foil on the workpieces, but, according to expert judgment, it can be taken approximately equal to 10% of the thickness of the copper foil $\left(\sigma_{etch} \sim \frac{h}{10}\right)$.

(12) $$N_{etch} \in N\left(w_r, \frac{h}{10}\right).$$

Now it is possible to determine the parameters of the distribution law of conductor's lower part (13), which will take into account the influence of the processes of exposure and etching together. For this, it is necessary to consider the composition of their distributions [12].

(13) $$N_w \in N(M_w, \sigma_w) = N\left(w_r, \sqrt{\frac{2*{\xi_{exp}}^2}{36} + \frac{h^2}{100}}\right).$$

Now we can transform the obtained distribution law N_w so that it takes into account the etching factor. To achieve this, we move from considering the width of the lower base of the conductor to the cross-sectional area.

We suppose that during the manufacturing process, the width of the conductor can change by the amount Δw, then the area of the conductor can be represented in the following form (14).

(14) $$S_{model}(w_r, h, F) = \frac{w_t + (w_b + \Delta w)}{2} * h = \\ = \left(w_r - \frac{h}{F}\right) * h + \Delta w * h.$$

An additional term allows determining the type of transformation of the standard deviation for the distribution law N_w. Therefore, the final form of the distribution law will be as follows)15)

(15) $$N_w \in N(M_S, \sigma_S) = \\ = N\left(S_{model}(w_r, h, F), \left(\sqrt{\frac{2*{\xi_{exp}}^2}{36} + \frac{h^2}{100}}\right) * h\right).$$

Based on IPC-6012B [10], the limiting reduction in conductor cross-sectional area cannot exceed 20%. We also introduce an additional restriction on the increase in the cross-sectional area, due to the fact that an increase in the cross-sectional area in this case is equivalent to a decrease in the distances between the conductors. Therefore, a conductor will be considered defect-free, if the cross-sectional area lies in the interval $(0{,}8 * S_{ideal}; 1{,}2 * S_{ideal})$. Taking into account the above, we can determine the probability of a defect-free conductor exit using the Laplace function (16).

(16) $$P_w\{0{,}8 * S_{ideal} \le S \le 1{,}2 * S_{ideal}\} = \\ = \Phi\left(\frac{1{,}2*S_{ideal} - M_S}{\sigma_S}\right) - \Phi\left(\frac{0{,}8*S_{ideal} - M_S}{\sigma_S}\right).$$

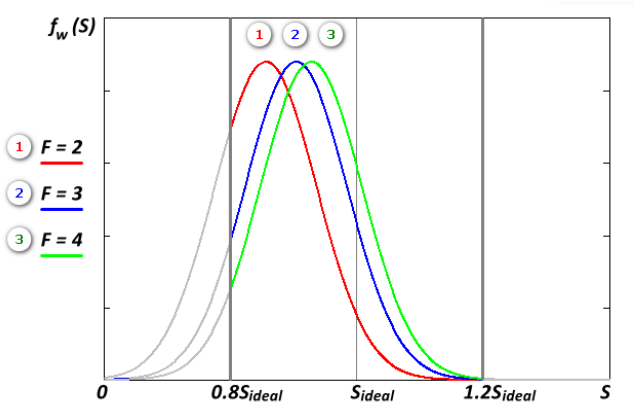


Fig.8. Graphic representation of formula (16) with different etching factors

The resulting expression (16) can be interpreted as the area of the figure, which is limited by the distribution density function $f_w(S)$ and the OS axis, as well as vertical lines passing through the values $0{,}8 * S_{ideal}$ and $1{,}2 * S_{ideal}$. An example of such a graphical representation is shown in the

Figure 8. As we can see, with an increase in the etching factor *F*, the area of the figure in a given range increases.

Now we can similarly find the probability of getting a gap between the conductors. Since the absence of a defect is considered to be a decrease in the width of the gap by 20% [10], applying the conclusions outlined to determine the quality of the conductor, it is possible, on the basis of (13), to draw up a distribution law that will describe the process of creating a gap (17) and the probability of creating a defect-free gap (18). Since it is initially intended to create a conductor in an optimal etching process($w_b = w_r$), then the probability of obtaining the desired gap does not depend on the etching factor, but depends only on the accuracy of the exposure process and the thickness of the copper foil.

$$N_{clr} \in N(M_{clr}, \sigma_{clr}) = N\left(w_{clr}, \sqrt{\frac{2*\xi_{exp}{}^2}{36} + \frac{h^2}{100}}\right). \quad (17)$$

$$P_{clr}\{0{,}8 * w_{clr} \le w_{clr} \le 1{,}2 * w_{clr}\} = \quad (18)$$
$$= \Phi\left(\frac{1{,}2*w_{clr} - M_S}{\sigma_{clr}}\right) - \Phi\left(\frac{1{,}2*w_{clr} - M_{clr}}{\sigma_{clr}}\right).$$

Based on the obtained expressions, we can draw up a formula to determine the probability of good PCB $P_{pcb}(w_b, w_r, w_{clr}, h, F, \sigma_{exp}, \sigma_{etch})$ taking into account its geometric parameters: width of the track, width of the gap and the thickness of the copper foil, as well as parameters of the technological processes of its manufacture: errors at the stage of exposure and etching. Since the events that describe the functions are independent, to get the aggregate function P_{pcb} it is necessary to multiply the obtained probabilities P_w and P_{clr} (19).

$$P_{pcb} = P_w\{0{,}8 * S_{ideal} \le S \le 1{,}2 * S_{ideal}\} * \quad (19)$$
$$* P_{clr}\{0{,}8 * w_{clr} \le w_{clr} \le 1{,}2 * w_{clr}\}. \quad (20)$$

The resulting equation allows the adjustment of the ranges that set the boundaries for changing the parameters. For example, in the PCB manufacture of the first and second classes according to the IPC-A-600G standard [11], the maximum possible changes in the cross-sectional area of the conductor and the gap width can be increased up to 30%, and, conversely, in the manufacture of particularly reliable devices, the ranges can be narrowed.

We construct a family of curves showing the dependence of the probability of defect-free PCB production on the width of the photoresist covering the conductor at various copper layer thicknesses and etching factors (Figure 9). The graphs are constructed taking into account the following restrictions: optimal etching process is considered and width of the conductor is equal to the size of the gap ($w_r = w_b = w_{clr}$).

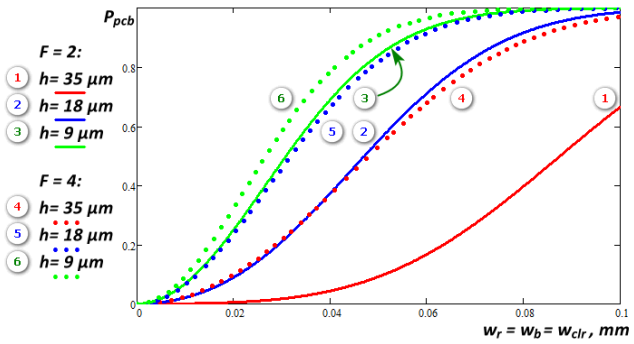


Fig.9. Probability of defect-free PCB production, depending on the width of the photoresist covering the conductor for various parameters

In general, the obtained results are consistent with the previously obtained quality function *Q* (Figure 5). The plotted curves allow obtaining information on the advisability of manufacturing PCB using a particular technological process. So, for example, it is difficult without defects to make PCB with 0.1 mm tracks, copper 35 µm thick in production with an etching factor of 2 ($P_{pcb} = 66\%$, curve 1, Fig.9), but by improving the production process by increasing the pickling factor ($P_{pcb} = 97\%$, curve 4, Figure 9) or by reducing the thickness of the foil ($P_{pcb} = 99\%$, curve 2, Figure 9), we can achieve the desired result.

Discussion

The developed model does not take into account the effect of the length of the conductors on the probability of a good PCB output, depending on the length of the conductors or on their number, since additional experimental research is required to introduce these parameters into the model, since it is impossible to accurately answer the question: “will there be 2 conductors of short conductors more reliable than 1 long?"

This study is the basis for future work to assess the impact of other design parameters and technological stages of creating PCB on the final probability of a defect-free product. For example, we can determine the effects of the pressing process depending on the thickness of the dielectric layers and the amount of copper on the layers, or the minimum via diameter for PCB of a given thickness.

Taking into account the development of the fields of machine learning and big data, the created model can be used to proactively identify equipment failures, explore opportunities for improving the technological process and create a system for continuous quality control of products.

Conclusion

As a result, a model was obtained that reflects the dependence of the probability of a defect-free PCB on the parameters of the design and the technological process used for its manufacture and including exposure and etching. The advantages of the model include its ease of use and the possibility of supplementing with other factors and process models that can affect the quality of PCB, for example, drilling and pressing. It is also worth noting that the addition of the model is possible using theoretical and experimental dependencies. Therefore, the model is convenient to use as a basis for further development and refinement. At the same time, the model can be simplified by excluding parameters that do not need to be considered. The use of the elements of the theory of probability in the description of the model allows not only aggregating the influence of various factors, but also provides an opportunity to build connections between them.

From a design point of view, the results obtained make it possible to assess the quality of PCB at a stage in advance, taking into account the availability of information about the technological process, as well as to quantitatively compare the quality of PCB with each other in the presence of the same production process. From the point of view of production, the use of the resulting model will allow estimating the labor intensity of manufacturing PCB and, accordingly, adjust their cost and reduce the number of defective products.

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***Authors**: Associate Professor Fedor Vasilyev, PhD in Technical Sciences, Head of the Department of Digital technologies and information systems, Moscow Aviation Institute (National Research University), Volokolamskoe Highway, 4, Moscow, Russia, E-mail: fedor@niit.ru*
Assistant Vladimir Isaev, Department of Digital technologies and information systems, Moscow Aviation Institute (National Research University), Volokolamskoe Highway, 4, Moscow, Russia, E-mail: isaevtver@gmail.com
Assistant Maksim Korobkov, Department of Digital technologies and information systems, Moscow Aviation Institute (National Research University), Volokolamskoe Highway, 4, Moscow, Russia, E-mail: josef_turok@bk.ru

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