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A hybrid device for the acquisition of electrical tomography measurement data

Abstract. *The hybrid device for measuring data acquisition from electric tomography is used to monitor the level of moisture in the walls, however, due to the universality of the measurement method, it can also be used for objects with different electrical properties. As the name suggests, the hybrid tomograph is designed to combine two measurement methods (EIT impedance measurement methods and ECT capacitance measurement methods). The device has been equipped with current and voltage phase shift measurement systems at individual measuring points. The main problem in the design of measuring devices based on EIT technology is to ensure the correctness of current regulation in a wide range of impedances of the measured objects while maintaining minimum values of forced voltage and ensuring an optimal signal-to-noise ratio. Unlike its predecessors, the hybrid version 2.0 was based on the complex FPGA Altera Cyclone IV and Cyclone V, which in turn allowed us to use parallel function blocks independent of each channel. The measuring roles have been divided into eight systems.*

Streszczenie. *Hybrydowe urządzenie do akwizycji danych pomiarowych z tomografii elektrycznej służy do monitorowania poziomu wilgoci w ścianach, jednak ze względu na uniwersalność metody pomiarowej może być również stosowane w przypadku obiektów o różnych właściwościach elektrycznych. Jak sama nazwa wskazuje, tomograf hybrydowy ma za zadanie połączenie dwóch metod pomiarowych (metody pomiaru impedancji EIT i metody pomiaru pojemności ECT). Urządzenie zostało wyposażone w układy pomiaru przesunięcia fazowego prądu i napięcia w poszczególnych punktach pomiarowych. Podstawowym problemem przy projektowaniu urządzeń pomiarowych opartych na technologii EIT jest zapewnienie poprawności regulacji prądu w szerokim zakresie impedancji mierzonych obiektów przy zachowaniu minimalnych wartości napięcia wymuszonego i zapewnieniu optymalnej wartości sygnału do szumu stosunek. Hybrydowa wersja 2.0 w przeciwieństwie do swoich poprzedników została oparta na układzie FPGA Altera Cyclone IV i Cyclone V, co z kolei pozwoliło nam na użycie równoległych bloków funkcyjnych niezależnie od każdego kanału. Role pomiarowe zostały podzielone na osiem układów. (**Hybrydowe urządzenie do akwizycji danych pomiarowych z tomografii elektrycznej**)*.

Keywords: electrical impedance tomography, electrical capacitance tomography, sensors.
Słowa kluczowe: elektryczna tomografia impedancyjna, elektryczna tomografia pojemnościowa, sensory.

Introduction

The hybrid 2.0 device is intended to be used to monitor the moisture content of walls, however, due to the universality of the measurement method [1], it can also be used for objects with different electrical properties. As the name suggests, the hybrid tomograph is designed to integrate two measurement methods (impedance measurement method eit, and capacitance measurement method ect). The first versions of the hybrid tomograph were based on microprocessor systems, the measurements were performed sequentially on 8/16/32 channels and the sampling rate oscillated at the level of 100kSps, the measurement with the capacitive method was carried out independently (sequentially) from the impedance method which resulted in a significant extension of the measurement time. In the further stages of project development, there was a need to create a faster version. The hybrid version 2.0, unlike its predecessors, was created based on the Algae Cyclone IV and Cyclone V FPGA chip system, which in turn allowed us to use parallel function blocks independent of each channel. The measuring roles are divided into 8 Cyclone IV systems, one for four measurement inputs which are coupled with the ADS8588 multi-channel A / D converter and 0V signal exceedance detection systems have a measuring function. The signal so measured is then partially filtered using the FIR2 filter, then the RMS voltage and the phase shift of the signal between the excitation current and the voltage are calculated. In principle, the system is to be used to measure the moisture of walls, but due to the universality of the measurement method can find its application in studying the structure of many other non-dielectric objects [2-19]. Optimization methods use such methods as [20-32].

Development of a 4-channel measuring card

The work on the measuring block began with the development of a four-channel measuring card using a programmable logic system. This card contains the basic elements needed to perform the correct impedance measurement of the object. As the source of the excitation signal, two fast DAC converters were used with which the FPGA system generates the excitation signal with a given amplitude. One of the systems serves as the signal source, the other one is used to adjust the amplitude of the excitation signal. The signal thus prepared is transmitted to the current measuring block which, together with the ADC converter, creates a feedback loop for regulation. The current value is controlled by the FPGA system which sequentially checks the correctness of the current value. If it is correct, the measurement is made on the channels that are not involved in the signal forcing process. Data collected in this way is saved in individual RAM memory for each channel. Simultaneously with the start of data collection, the function block calculating the rms value of the measured signal begins to work. Thanks to the use of specialized function blocks, it is possible to obtain the calculated value of 2 periods of the clock signal after the data collection by the measuring block has been completed. The data measured in this way is transferred to the next ram memory, then the sequencing block switches the excitation signal to the next pair of electrodes using the multiplexer. Such a process is carried out cyclically, after completing a whole series of measurements, a flag is displayed informing HPS about readiness of data to be downloaded and the measurement process begins again. In the HPS Processor, after receiving information on the readiness of data, the functions performing data transmission from the computer via Ethernet or RS232 are called. The FPGAs used, due to the possibility of performing many operations at the same time, significantly accelerate the measurement process, the element limiting the measurement speed is the need to collect samples from at least one excitation signal period for a given electrode configuration at an excitation frequency of 1Khz, lasts 1ms

x 4 channels = 4ms. The impact of the data processing and transmission process has no noticeable effect on the speed of work. Below is a block diagram of the 4-channel system operation.

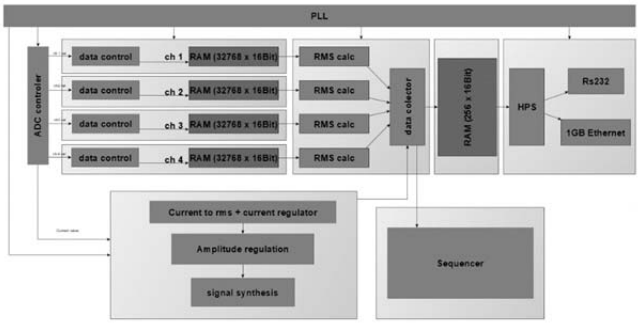

Fig. 1. Block diagram of the measuring system operation.

Below is a picture of a 4-channel system with a development board with an Intel Altera Cyclone V FPGA chip.

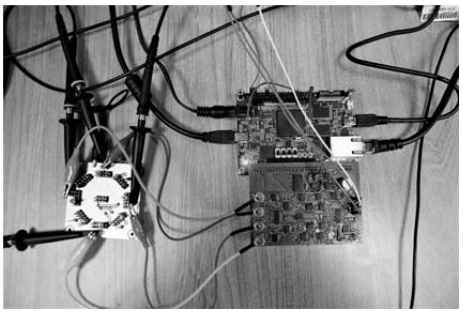

Fig. 2. 4-channel system with a development board with an Intel Altera Cyclone V FPGA chip.

Development of the measuring card

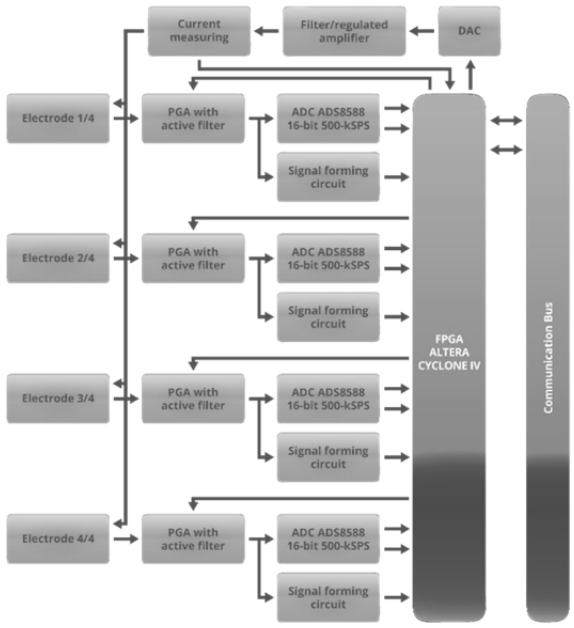

Fig. 3. Block diagram of the measuring card.

The measuring card consists of four active electrodes containing blocks forming the measured signal along with gain control and zero point detection of the measured voltage. Together with the FPGA Cyclone IV system and ADC converter it performs a measuring function. The signal filtration process, calculation of RMS value, signal phase measurement takes place there, then the data prepared in the way via buses is forwarded to the control unit. Below is the block diagram of the measuring card.

The signal measured through amplifiers with high input impedance is transmitted to the system of measuring amplifiers with adjustable gain and then in order to reduce the effect of interference resulting from 50 Hz on the high-order active third-order filter. Then the amplified and filtered signal is transmitted to the zero point detection system consisting of a set of compensated comparators by means of which the sinusoidal signal is transformed into a rectangular one with an amplitude acceptable for the inputs of the FPGA system. The electrical diagram of the measuring card input block is shown in Fig.3.

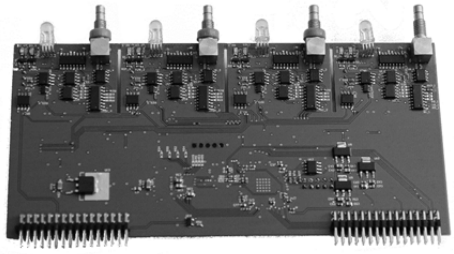

Fig. 4. Measurement card after assembly.

Development of the central unit of the device

The mainboard performs the data and address functions of the individual blocks, additionally on the main board there is a power supply unit that converts voltage from a constant voltage of 12V (battery) to + 5V, +15, -15, 3.3V, 1.2V, 2.5V respectively required for correct operation of individual function cards. In addition, the battery control and charging system is integrated in the power supply unit. One of the other functions that the motherboard performs is the generation of a forced current signal together with the signal correctness control system and checking the quality of the electrode connection.

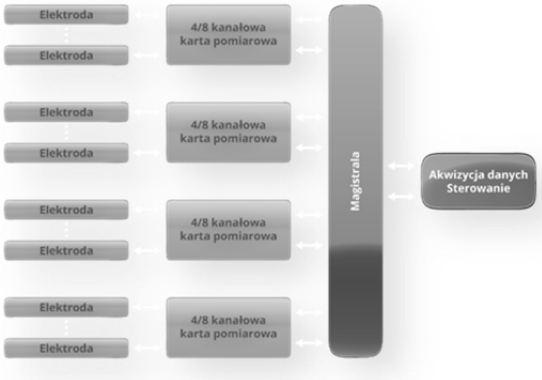

Fig. 5. Block diagram of of the motherboard layout.

Due to the logic of the system's operation, the power generation block has been placed on the motherboard. Due to the requirements for a wide measuring range of the system, it must ensure a minimum uncertainty of forced current regulation. It was built based on two DACs. One is the function of the signal generator and the other serves to adjust the amplitude value of the forced signal. The adjustment process takes place via the digital feedback loop implemented inside the fpga system, similarly to the case of the measuring cards, the Intel Altera Cyclone IV EP4CE10 chip was used. This solution allows for full control over both the value and the shape of the excitation current so that it allows the use of signals of various shapes as the excitation signal. The block diagram of the motherboard layout is shown below.

Additionally, the main board has a zero point detection system for the current value from which the signal transmitted via the signal forming block goes to the measuring cards as a reference to the phase shift measurement.

Development of a control and data processing unit

The data controller was built on the foundation of the de0 nano soc board containing the Intel Altera Cyclone V fpga chip which, in addition to fpga blocks, has a built-in two-core Cortex A9 processor. The control and measurement system collects data from individual measurement cards via fpga blocks, transfers configuration data to individual measurement blocks and supervises the correctness of measurements. The user interface along with reconstruction mechanisms is performed by the processor along with the Linux system

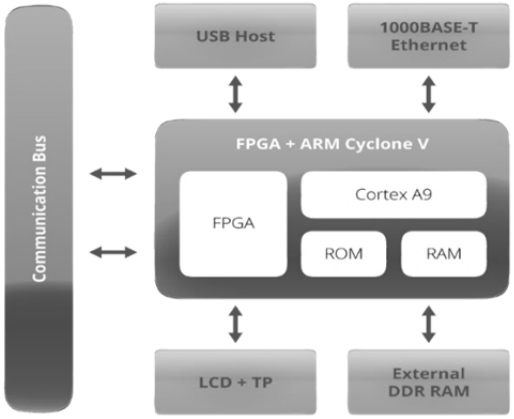

Fig. 6. Block diagram of the device.

Communication between the supervisory unit and individual system components takes place via parallel buses (address and data) to which virtual RAM memories have been connected on the side of individual components. Individual cards have their own individual addresses, thanks to which the data controller has been provided with access to data as one consistent RAM memory. Four less significant bits in addressing data are used to select the memory cell from which the data are to be downloaded, while the 3 above to select the card number. Due to the need to address 128 bytes, the 8-bit address bus has not been used. The diagram below shows how to connect the signals of individual system components.

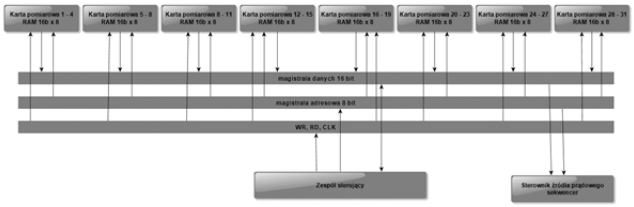

Fig. 7. Block diagram of connection the signals of individual system components.

Individual measuring cards, after detecting their individual address on the address bus, switch data lines from the high impedance state to the output mode connected to the data memory of the ram, thanks to which the control unit gains direct access to the measured data in individual measuring cards. The way of communication with the parallel ram memory is presented below. The desired data appears on the data bus in the second clock signal period after setting the address on the selected card.

Device tests

The first work on starting and testing the device took place on the table. As a measurement phantom, a test element was used. It is a board containing 32 leads connected with each other with a set of resistors allowing for testing the correctness of the device operation.

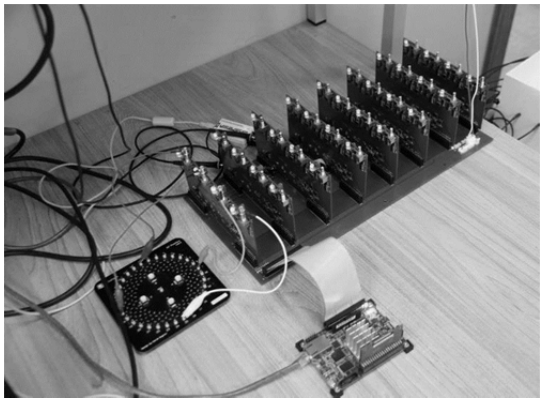

Fig. 8. Works on starting the CT system, first attempts of measurements on a resistive phantom.

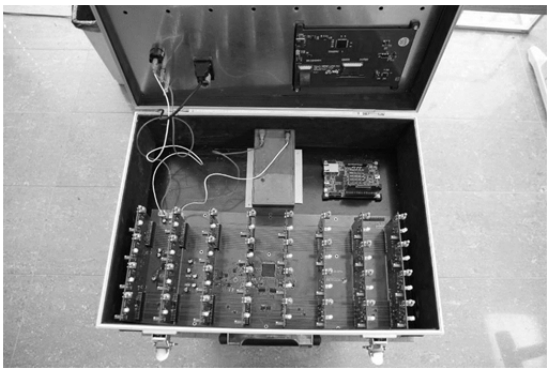

Fig.9. Appearance of the device during assembly.

In the next stage of work, the device was tested in terms of correctness of current regulation and electrical compatibility with measuring electrodes on the real object

Fig. 10. Hybrid tomograph 2.0 to use the tomograph to measure the test wall.

Conclusion

This article presents the construction of a hybrid tomography 2.0 based on electric tomography. The device can be used to measure objects with different electrical properties. The hybrid tomograph is designed to combine two measurement methods, impedance measurement method and ECT capacitance measurement method. The device has been equipped with current and voltage phase shift measurement systems at individual measuring points.

The presented solution was based on Altera Cyclone IV and Cyclone V FPGA processors, which in turn allowed the use of parallel function blocks regardless of each channel. The device has been equipped with current and voltage phase shift measurement systems at individual measuring points. The correctness of current regulation in a wide range of impedances of measured objects has been ensured while maintaining the minimum values of the applied voltage and ensuring an optimal signal to noise ratio.

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