

Low Voltage and Wide Bandwidth Class AB Variable Gain Amplifier in 0.18- μm CMOS Technology

Abstract. Variable gain amplifier (VGA) is the key element for amplifying process in analog to digital converter (ADC). In this paper, a low voltage and wide bandwidth class AB VGA is designed using CEDEC 0.18- μm CMOS process for high speed applications. The result show that, the designed VGA has a wide bandwidth of 100-MHz and consumes power less than 125 μW at 1V supply voltage. From the results it is also evident that the circuit is capable of working with high linearity and wide bandwidth. The frequency response (Gain) and the wide bandwidth of this class AB VGA is better than previously reported class AB VGA. Smaller transistors are used to make the chip small and it occupies only 0.003 μm^2 . Such a VGA is suitable for high-performance RF devices.

Streszczenie. W artykule opisano niskonapięciowy, szerokopasmowy wzmacniacz klasy AB typu VGA (variable gain amplifier – wzmacniacz o zmiennym wzmacnieniu). Wzmacniacz zaprojektowano wykorzystując proces 0.18 μm CMOS. Wykonano wzmacniacz o pasmie 100 MHz i poborze mocy mniejszym niż 125 μW przy napięciu zasilania 1 V. (Niskonapięciowy, szerokopasmowy wzmacniacz klasy AB typu VGA w technologii 0.18 μm CMOS)

Keywords: CMOS, Class AB, High speed, Low Voltage, Variable Gain Amplifier (VGA).

Słowa kluczowe: wzmacniacz klasy AB, wzmacniacz VGA – wzmacniacz o zmiennym wzmacnieniu.

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Introduction

Variable gain amplifiers (VGA) are one of the most significant components in wireless communication receivers [1]. In typical communication receivers, VGAs are normally used in a feedback circuit to supply steady signal to baseband analog-to-digital converter (ADC) for random strength of received signal realizing the function of an automatic gain control (AGC). Gain range, power consumption and bandwidth of an ADC are strongly influenced by the performance of operational amplifier. In low voltage applications like wireless communication, mobile imaging applications etc. high-performance VGAs are one of the most essential design blocks [1-2]. Usually, VGAs are signal-conditioning amplifiers having electronically configurable voltage gain. VGAs are currently available from dc to gigahertz frequency signals in different I/O configurations. The current applications of VGAs are ranging from ultrasound, radar, lidar etc. to different types of communication devices. Even in speech analysis equipments VGAs are widely used in order to enhance dynamic performance [3]. At present, the key design aspects for VGA, like other circuits, are the low power dissipation, wide bandwidth and low cost as well [4-5]. Indeed, class AB has become very significant alternative for any application requiring VGA over the last few years [5-6].

As utilized in low power devices, power supply voltage and power dissipation of VGAs should be kept as low as possible [6]. Rapid developments of process technologies make the permissible maximum supply voltage gradually scaling down [7],[8]. It is observed that almost all integrated circuits within low power range operate with supply voltages between 1 V to 1.8 V [8],[9]. Design a highly linear VGA with wide bandwidth and less power dissipation at such low supply voltages is really very challenging. As VGAs are typically have to retain high linearity and low noise over the total bandwidth and gain range, therefore, it is also imperative to maintain constant bandwidth with varying voltage gain. This is possible to obtain by using current-mode techniques [10].

A number of class AB VGA designed so far, described in different literatures, with high linearity, wide bandwidth at acceptable power dissipation range. However, researchers experienced gain limitation issues in wide bandwidth and the transistor's size [11]. This paper presents a VGA design

with improved characteristics to the circuit proposed in [11]. This design overcomes the limitations of the conventional class AB VGA through the application of Current mode technique. Small size of transistor is used in this design to reduce the size of circuit and cost as well. The circuit proposed in this paper operates in class-AB mode and show better performance than its forerunner (class-A), specially, in perspective of signal dangle and linearity as well as preserving the identical static power dissipation and die area [12-13].

Two-stage cascade variable gain amplifier

The proposed VGA design illustrated in [11] run at small supply voltage having low power dissipation with high bandwidth as well as occupying very small chip area. Fig. 1 shows the architecture of VGA in [11], which is a two stage cascade structure, composed of a linear transconductor amplifier along with a linear transimpedance amplifier with feedback through shunt resistors (R_f).

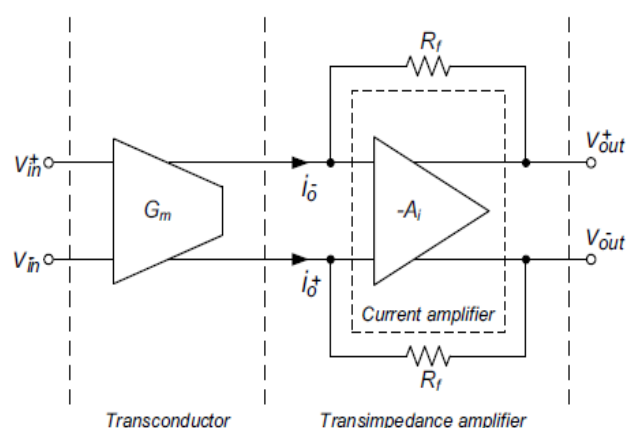


Fig.1. Architecture of the proposed VGA stage in [11]

The voltage gain of the VGA in Fig. 1 is the multiplication of transconductance gain (G_m) and transimpedance gain (R_m). The transimpedance gain (R_m) of the amplifier [11],[14] is given as

$$(1) \quad R_m = -\frac{(R_f A_i - R_{in})}{(1 + A_i)}$$

where, R_{in} and A_i represent the input resistance and the current gain of the current amplifier respectively. It should be noted that, if $A_i \gg 1$, we get $R_m \approx -R_f$. Hence, a linear transconductance gain (G_m) and a high-gain current amplifier are needed to design a highly linear VGA. The schematic of the VGA [10] in CMOS technology is given in Fig. 2. This circuit has disadvantage of bandwidth limitation (restricted to 50MHz) and big size transistors are also used.

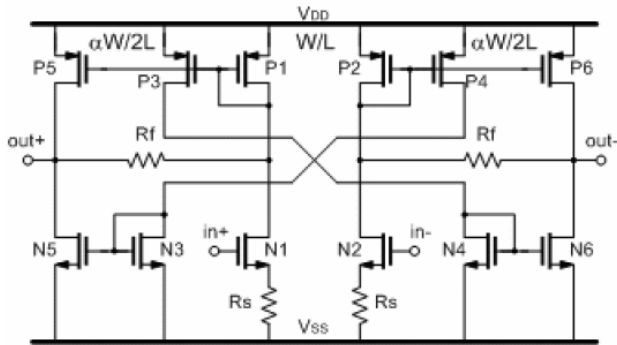


Fig.2. Circuit realization of the proposed circuit [11] with CMOS.

Two-stage cascade variable gain amplifier

Fig. 3 depicts the schematic of the proposed VGA that is a combination of a source degeneration differential input transconductance amplifier (N1 – N2, R_s) and a current-mode transimpedance amplifier (P1 – P6, N3 – N6) in desire of maximizing transconductance, bias current efficiency and minimizing supply voltage and noise as well [15],[16]. Cascaded current mirrors usually implement the DC current sources. Such structures possess a serious disadvantage; they are not capable of discarding common-mode signals.

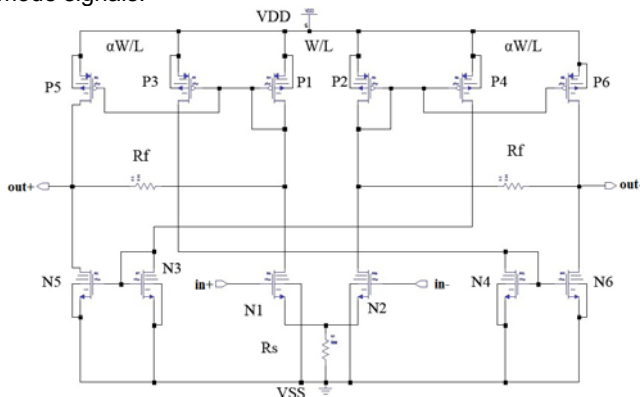


Fig.3. Schematic of the proposed VGA with class-AB output stage and signal feed forward topology.

The second stage current amplifier (P1 – P6, N3 – N6), based on mirror, settles this problem utilizing feed forward technique that permits differential signals to be constructively united while simultaneously cancel common-mode signals [17]. This type of current amplifier when joint with feedback resistance (R_s) forms a transimpedance amplifier essential for the conversion of current into voltage. Furthermore, such output stage also offers a class-AB operation of the amplifier and allow larger signal swing in comparison to its ancestor presented in [18]. Thus the key merit of such VGA circuit is its capability to yield splendid signal linearity without giving up original advantages of the power dissipation and circuit simplicity.

It is important to note that the size of each transistor is reduced according to the ratio (W/L) to get a smaller size of IC. Besides, the number of resistor R_s that have been used in previous circuit is also reduced from 2 to 1. Table I shows the comparative sizes of transistors used in this work and in previous work.

Table 1. VGA transistor size comparison

Transistors	W/L ($\mu\text{m}/\mu\text{m}$) [10]	W/L ($\mu\text{m}/\mu\text{m}$) This work
N1 – N2	1.5/0.18	1.5/0.18
P1 – P2	10/0.5	3.6/0.18
P3 – P6	25/0.5	9/0.18
N3 – N6	5/0.5	1.8/0.18

A small-signal transconductance gain (G_m) [10],[13] of the first stage is expressed as

$$(2) \quad G_m = \frac{(g_{in})}{(1 + g_m R_s + s R_s C_{gs})}$$

Where g_m and C_{gs} represent transconductance and gate source capacitance of N1 and N2 respectively. The differential current gain A_i and input resistance R_{in} [11],[14] of the amplifier is given by

$$(3) \quad A_i = \frac{g_{mx}}{g_{mi} + s C_x} \left(1 + \frac{g_{my}}{g_{my} + s C_y} \right)$$

and

$$(4) \quad R_m = \frac{1}{(g_{mi} + s C_x)}$$

Where g_{mi} , g_{mx} and g_{my} are transconductance of P1 – P2, P3 – P6 and N3 – N6 respectively. C_x and C_y are corresponding total capacitance (referred to ground) at gates of P1 (P2) and N3 (N4) which are chiefly attained from transistor gate-source capacitances. At low frequencies, since $g_{mx} = g_{mi} (\alpha/2)$, thus differential current gain (A_i) of Fig. 2 equals to α , which is similar to what we get from the original circuit in Fig. 2. Thus, by substituting (3) and (4) into (1), the equation of small-signal transimpedance gain [11],[14] obtained to be

$$(5) \quad R_m = -\frac{\alpha \left[2R_f - \frac{1}{g_{mx}} + s \frac{C_y}{g_{my}} \left(R_f - \frac{1}{g_{mx}} \right) \right]}{2 \left[1 + \alpha + s \left(\frac{C_y}{g_{my}} \left(1 + \frac{\alpha}{2} \right) + \frac{C_x}{g_{mi}} \right) + s^2 \frac{C_x C_y}{g_{mi} g_{my}} \right]}$$

The feedback resistor (R_f) is responsible for setting voltage gain range while source degeneration resistance (R_s) is tuned for varying the amplifier gain. The lowest magnitude of the resistance R_s sets the highest value of the gain for a specific gain range (set by R_f) and it also determines the highest static current drawn by the VGA. The same procedure proposed in [19],[20] can also be utilized to tune the grounded resistor (R_s).

Results and discussions

The proposed class AB VGA circuit with a 1V power supply voltage is designed and simulated in CEDEC 0.18- μm CMOS process. With $\alpha = 5$, transistor sizing of the VGA circuit is listed in Table I. In this design, the minimum value of 500 Ohms of R_s is to be chosen for ensuring that the maximum power dissipation not exceeds 120uW for a bandwidth over 100MHz.

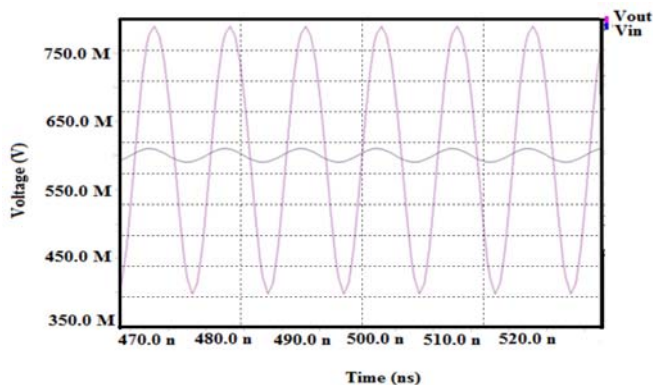


Fig.4. Simulation result of output swing at maximum voltage gain of 26 dB for 1V power supply.

By using a transient analysis within Mentor Graphics design architect IC (DA-IC), Fig. 4 shows the input and output signals for the maximum (26dB) voltage gain.

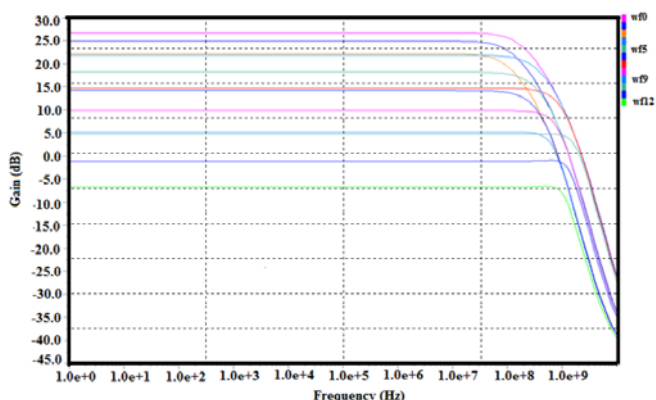


Fig.4. Frequency response of the VGA where Rf: 500k Ω , 150k Ω , 50k Ω , 15k Ω and Rs: 500 Ω , 5k Ω , 15k Ω .

Fig. 5 shows four families of curves of obtained gain response, which was obtained by varying the value of feedback resistor (Rf) from 15k to 500k. This renders common gain tuning of the amplifier, where highest gain and lowest gain are achieved with Rf = 500k, and Rf = 15k, respectively. Within each family of curve (wf0 –wf12), the value of Rs was varied to achieve finer tuning of gain. It is observed that voltage gain control at constant bandwidth can be obtained by changing Rs; on the other hand changing Rf influences the bandwidth of the VGA since Rf sets the leading output pole frequency of the circuit. Therefore, for designing the VGA, Rf should be selected first in accordance with the requirement of bandwidth after that Rs is to be tuned to conform the voltage gain.

Table 2. VGA PERFORMANCE COMPARISON

Parameters	[10]	This work
Technology	Spectre 0.18 μm CMOS Technology	CEDEC 0.18 μm CMOS Technology
Bandwidth	~50 MHz	~100 MHz
Gain range at constant bandwidth	25 dB	26 dB

A comparative study of class AB VGA between this work and the work in [10] is depicted in Table II. From the table, it is evident that the circuit is able to vary the voltage gain in linear dB from -7 to 26 dB. The total power consumption is less than 125uW from a 1 V power supply having a wide and constant bandwidth, which is better than reported in [10]. Table II also sum up the overall performance of the class AB VGA. It is, therefore, clear that the proposed class AB VGA achieve the same gain range as before, while it is

operated with lower supply voltage and smaller size transistors.

The layout of the modified class AB variable gain amplifier (VGA) circuit is also designed in CEDEC 0.18- μm CMOS process. In Figure 6, the complete chip layout of the modified class AB VGA is shown. In this layout, the resistors are excluded from the model circuit and are replaced with an external resistor component. It is because of drawing a resistor layout with high resistance value in the chip layout is not that practical as the area of the chip will be very big which will result in a large die size and high cost for chip to tape out. In this research, the size for each cell of the MOS transistors in class AB VGA circuit is made smaller, which implies that the size of the modified class AB VGA circuit is smaller than its ancestor. It occupies only 0.003 μm^2 of silicon space.

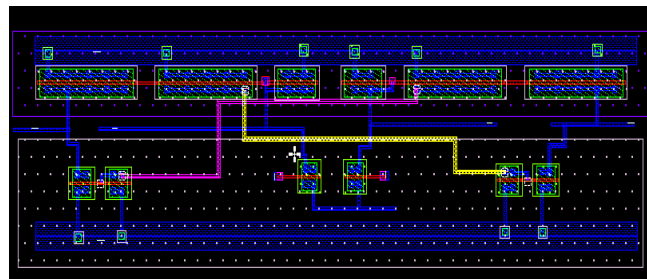


Fig.6. layout design of class AB variable gain amplifier.

Conclusion

A compact design of modified class-AB variable gain amplifier in CEDEC 0.18- μm CMOS process using two stage cascade-like structures consisting of a linear transconductor amplifier followed by a current amplifier-based feedback transimpedance amplifier is demonstrated in this paper. In this design, small design parameters were used to reduce the die size of whole chip. The parameters of the VGA are also compared with previous tasks and it has been found that the circuit is capable of achieving high linearity and wide bandwidth at a smaller chip area compared to the previous work. The results also verify that the utilization of current mode in amplifier circuit, the voltage gain can be tuned while keeping the bandwidth constant.

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